The Effect of Wire Length Minimization on Yield

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Abstract

Wire length minimization (WLM) *has received significant attention in the compaction stage of* VLSI *layout synthesis. In most cases, reduction in wire length also results in better circuit yield. However, a trade-off may still exist between total wire length and yield. In* WLM *only the area/length of the layout patterns is considered whereas for yield enhancement both the area of the layout patterns and the spacing among them must be considered. The trade-off between these two features is analyzed on a set of benchmark layouts in this paper.*

1 Introduction

Wire-length minimization (WLM) is a commonly-used secondary optimization performed in the compaction stage of VLSI layout synthesis. Several algorithms have been proposed for WLM [8, 10, 11] and they have been implemented in commercial CAD systems. In compactors, WLM is performed by moving the non-critical (slack) elements after solving for minimum area. It is well known that wire length reduction can result in better electrical performance due to improvements in RC characteristics. It has been shown in [8] that significant wire length reduction can be achieved after compacting the layout. Wire length minimization can sometimes even lead to smaller area if layouts are compacted iteratively in both directions. Since compactors do not alter the topological order of the layout elements, further reduction in the wire length can be achieved only by changing the topological order of the layout elements before compaction. It is shown in [3] that up to 30% wire length reduction can be achieved by reassigning the nets to different tracks during the routing stage.

In most cases, reduction in wire length also results in better circuit yield [2]. However, a trade-off generally exists between reducing wire length and increasing yield. That is, large increases in yield can be achieved with modest increases in wire length. In wire length reduction only the area/length of the layout patterns is considered. For yield enhancement both the area of the layout patterns and the spacings among them must be considered. The trade-off between area and spacing depends on the defect densities of the open- and short-circuit type faults of the manufacturing process. The relative magnitude of these defect densities is technology dependent whereas the actual defect densities depend on the manufacturing facilities. We illustrate the similarities and the differences between these two optimizations in the following section.

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2 Wire Length Minimization vs. Yield

In WLM algorithms the primary objective is to minimize the area of the layout patterns so that the electrical performance of the final circuit is improved. Compactors, in the absence of WLM, place the layout elements as close as possible to one edge of the layout [1]. This generally results in unnecessarily long wire segments as shown in Figure 1b. When WLM is included, the unnecessary jog segments are removed from the layout as shown in Figure 1c. When the jogs are completely eliminated, most of the elements in the layout tend to be as close together as the design rules permit. Minimum spacings adversely affect yield, however, because short-circuit faults are more likely among tightly-packed elements. For instance, if the layout of Figure 1b is optimized for yield, the layout shown in Figure 1d results.

In WLM a segment is placed via a cost function that is weighted according to the orthogonal connecting segments at its two ends [7, 10]. For yield enhancement, the optimal location for a wire segment depends on (a) its length, (b) the spacings between it and adjacent elements, and (c) the elements connected on both ends and their widths [2]. For example, wire segment A in Figure 2a has 30 units of slack. If it is moved 30 units upward jog J1 can be completely eliminated. However, this is not an optimal location when yield enhancement is also a consideration. As shown in Figure 2b, the optimal location is 10 units below. If Segment A is moved further upward, the increase in the probability of short-circuit faults is higher than the decrease in the probability of open-circuit faults due to jog length reduction as shown in Figure 2c. In typical VLSI technologies, the defect densities for short-circuit type faults are much higher than those of open-circuit type faults [4]. Therefore, in order to achieve better yield characteristics, the proper distribution of free space among the layout elements is very critical.

For some elements in the layout the wire length remains the same irrespective of their positions. For example, wire segment A shown in Figure 3a is connected to two wire segments, one from the top and the other from the bottom. Therefore the total wire length of these two vertical wire segments is independent of the position of A. In such a situation, the position of segment A will not be altered during WLM. However, for yield enhancement, it will be placed in the middle as shown in Figure 3b to reduce the probability of a short circuit with the other elements in the same layer.

The amount of jog length justified for a wire segment depends on its length and on the spacing from the wire segments above and below. If the segment length is longer, the increase in open-circuit fault probability due to the additional jog length is easily offset by the reduction in short-circuit fault probability due to the increase in the spacing to its adjacent elements. This is illustrated in Figures 3c through 3e. In Figure 3e, wire segments A and B are longer compared to the wire segments C and D. Therefore, it is preferable to place these longer segments farther away from the wire segments E and F,

Probability of Failure (%)					
Failure Mode	Simple Compaction	Compaction with WLM	% Red.	Modified for yield	% Red.
M-1 Open	4.72	4.32	8.5	4.39	-1.6
M-1 Short	2.47	1.97	20.2	1.85	6.1
Wire Length (mm)					
M-1	1099K	958K	12.8	990K	-3.3

Table 1: Effect of WLM on yield during compaction.

respectively, when compared to segments C and D. If A and B were moved even further away, to uniformly distribute the spacing among segments A, B, E and F, longer jogs (J1, J2) would be required. This would result in a higher overall fault probability due to the additional jog lengths.

3 Examples

To illustrate the effect of WLM on yield, the yield analysis results for an industrial example are shown Table 1. The layout consists of thousands of transistors and has about 30% routing area. The layout is compacted using an IBM compactor [7]. The yield analysis tool XLASER [6] is used for estimating the probability of failure (POF) of the circuit. The second column of Table 1 shows the POF of the metal-1 layer of the layout generated with simple compaction. The third column shows the POF of the layout when wire length minimization is performed during compaction. As shown in the fourth column, the defect sensitivity of short- and open-circuit faults is reduced by 20.2% and 8.5%, respectively. This improvement is due to the 12.8% reduction in the wire length of the metal-1 layer. The layout was then modified for yield enhancement and the probability of failure due to short-circuit faults was further reduced by 6.1%. However, the fault probability of the open-circuit faults increased by 1.6% due to a 3.3% increase in the wire length that occurred during yield enhancement. It is to be noted that the defect density of short-circuit faults is often much higher (up to 5 to 10 times) than that of open-circuit faults [4]. Therefore, reducing short-circuit faults even at the expense of marginal increases in wire length can result in better layouts.

To illustrate the effect of wire length reduction on yield when the layout topology is modified during the routing stage of the physical design, a benchmark example has been analyzed and the results are shown in Table 2. Layout of the two-layer channel routing of *example 1* from [12] has been generated using the Magic CAD Tools [9] and analyzed for yield characteristics. By reassigning the nets to different tracks [3] the wire length of the vertical layer is reduced by 29.3%. The new layout is compared with the layout as per the original routing solution. The percentage reduction in the fault probability of open-circuit faults (29.2%) is almost the same as the percentage reduction in the wire length. However, the percentage reduction in short-circuit faults is much higher (51.3%). This is

Probability of Failure (%)						
	Shorts			Opens		
Layer	Orig.	Optim.	% Red.	Orig.	Optim.	% Red.
Vertical layer	2.24	1.09	51.3	3.53	2.50	29.2
Horizontal layer	2.48	2.10	15.3	3.61	3.55	1.7
Wire Length (mm)						
Vertical layer	9.81	6.94	29.3%			
Horizontal layer	11.31	11.09	2.0%			
Vias	57	34	40.4%			

Table 2: Effect of WLM on yield during routing.

not totally unexpected because the short-circuit fault probability of an element depends on its neighboring elements whereas its open-circuit fault probability is almost independent of its position. The reduction in the fault probability of short-circuit faults in the horizontal layer is a byproduct of changes in the adjacent tracks.

The topological changes lead to a significant reduction (40%) in the number of vias required to implement the routing as well [3]. Vias are eliminated by reassigning the net segments to the other layer. The very small reduction in the wire length of the horizontal layer is the result of the layer reassignment. The improvement in the defect sensitivity of the layout due to the reduction in the number of vias has not evaluated yet (due to a limitation of the available yield analysis tool). If the layout were to be subsequently compacted with yield enhancement as an objective, further improvements, as illustrated above, could be achieved.

4 Benchmark Results

To compare WLM with yield optimization, two-layer layouts have been generated for a set of channel routing benchmarks[12]. The layouts are scaled to 0.5 micron technology. All horizontal wire segments are assigned to the metal-1 layer and the vertical wire segments are assigned to the metal-2 layer (HV routing).

Each layout is first compacted vertically using [7] without WLM or yield optimization. The defect sensitivity of each layer for short- and open-circuit faults is estimated by using XLASER. Defect sensitivity is measured using the defect size distribution model [5] with $x_o = 0.5$, $p = 3.0$, and $q = 1.0$, and the defect densities are assumed to be equal for open- and short-circuit type faults. The defect sensitivities of metal-1 for short-circuit faults and metal-2 for open-circuit faults are shown in the third column of Table 3. (Sensitivities of the other layers are omitted for brevity.) Since the layouts have been compacted without automatic wire jogging, the wire length of the horizontal segments is not altered during compaction. Therefore, the defect sensitivity of the horizontal layer (metal-1) for open-circuit faults is essentially unchanged.

The layouts were then compacted by enabling either WLM or yield optimization. Algo-

Examples in [12]	Defect Type	No WLM POF	With WLM POF	% Red.	WL micron	With Yield Optimization POF	% Red.	WL micron	% Inc.
ex1	M1-S	0.001806	0.001783	1.27		0.001662	7.97		
	M2-O	0.002021	0.002008	0.64	1909	0.002020	0.05	1927	0.9
ex3a	M1-S	0.002479	0.002442	1.49		0.002403	3.07		
	M2-O	0.001829	0.001798	1.70	3346	0.001813	0.87	3379	1.0
ex3b	M1-S	0.002087	0.001992	4.55		0.001919	8.05		
	M2-O	0.002169	0.002138	1.43	4726	0.002152	0.78	4766	0.9
ex3c	M1-S	0.002219	0.002156	2.84		0.002108	5.00		
	M2-O	0.001944	0.001918	1.34	5473	0.001931	0.67	5519	0.8
ex4b	M1-S	0.001752	0.001667	4.85		0.001574	10.16		
	M2-O	0.001762	0.001719	2.44	6810	0.001739	1.31	6911	1.5
ex5	M1-S	0.001638	0.001570	4.15		0.001378	15.87		
	M2-O	0.001529	0.001508	1.37	6681	0.001541	-0.78	6855	2.6
Deutsch	M1-S	0.001328	0.001207	9.11		0.001145	13.78		
diff. ex.	M2-O	0.002005	0.001954	2.54	17711	0.001974	1.55	17919	1.2
Average	M1-S			3.68			8.42		
	M2-O			1.64			0.69		1.3

Table 3: Comparison of WLM with yield enhancement.

rithms for automatic yield optimization have been designed and implemented within the compactor of [7]. The defect sensitivities and wire length details with WLM are shown in the fourth and sixth columns and the corresponding results using yield optimization are shown in the seventh and ninth columns of Table 3. Under WLM the lengths of the vertical wire segments are reduced. Consequently, the defect sensitivity of the vertical layer is reduced on average by 1.6%. When the wire length of the vertical wire segments is reduced, the horizontal wire segments connected to them through vias are moved, and thereby the defect sensitivity of the metal-1 layer for short-circuit faults is reduced by 3.7%.

When the layouts are compacted with yield enhancement instead of WLM, the horizontal wire segments are moved such that the overall defect sensitivity of the layout is reduced. In this process the vertical wire segments might be stretched when compared to the WLM case. The defect sensitivity of short-circuit faults is improved by 8.4%, i.e., an improvement of 5% when compared with the WLM result. However, the increase in wire length of 1.3% in metal-2 resulted in a proportional increase in the defect sensitivity of that layer. Nevertheless the overall defect sensitivity of the layout is improved compared to the WLM result. The effect of the marginal increase in vertical wire length on performance is minimal. The defect sensitivity improvement can be directly translated into yield improvement with additional information on defect densities for short- and open-circuit faults, clustering factor data, etc. Our sample calculations show that an 8-10% improvement in defect sensitivity on 2 or 3 interconnect layers on a chip of 1 sq. cm can result in a 5-10% improvement in chip yield.

5 Conclusions

After minimizing the layout area during VLSI layout synthesis, there is freedom available to further optimize the layout for improved performance, yield, and manufacturability. Performance improvement using methods such as WLM is usually given priority over other improvements. It has been shown that layout modifications for yield enhancement also reduce wire length, which benefits performance. In the absence of criticality information, WLM (which is performed at the expense of yield enhancement) may not result in better circuits. On the other hand yield enhancement is always beneficial if the defect information is accurate, and the wire-length increase that occurs is minor. In practice these two optimizations can be selectively applied to various parts of the chip to result in designs that, overall, have higher yield and improved performance over those designed with standard methods.

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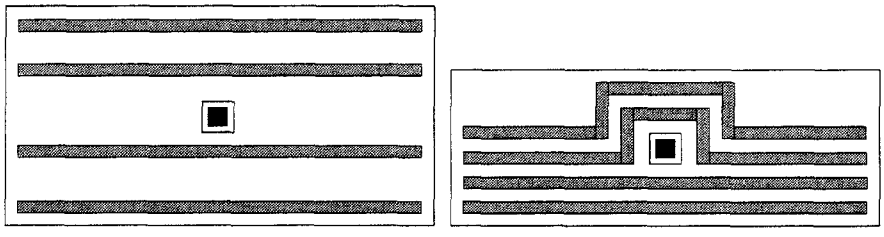
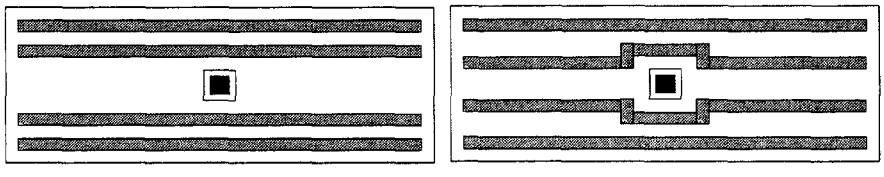


(a) Uncompacted layout.

(b) Compacted layout without wire length minimization.



(c) Compacted layout with wire length minimization.

(d) Compacted layout with yield enhancement.

Figure 1: Layout compacted with different options.

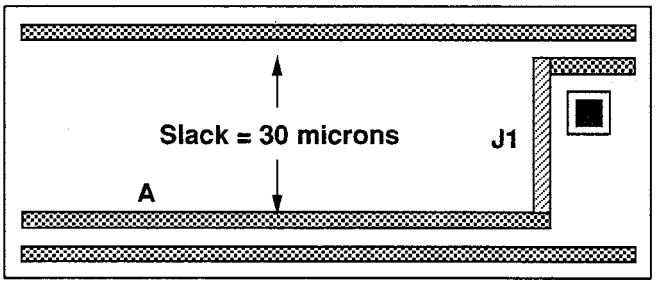


Figure 2a: Layout before relocating Segment A.

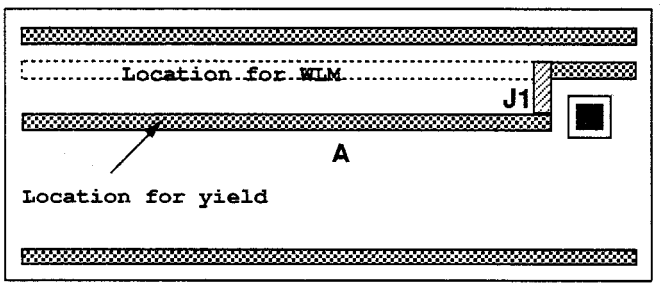


Figure 2b: Layout after relocating Segment A.

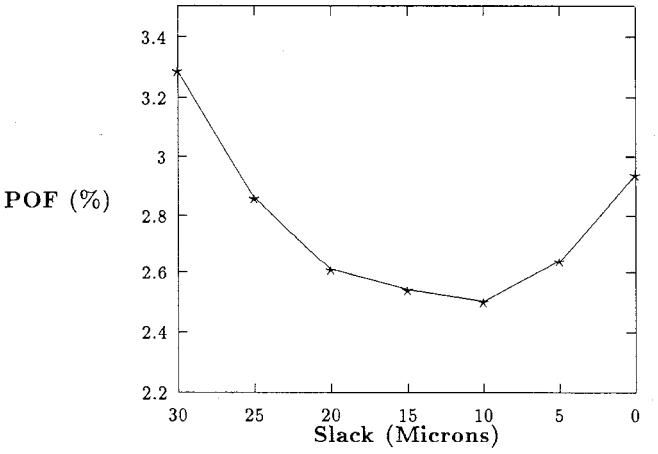


Figure 2c: Wire length minimization vs. POF for the layout shown in Figure 2a.

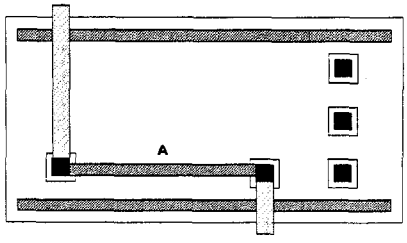


Figure 3a

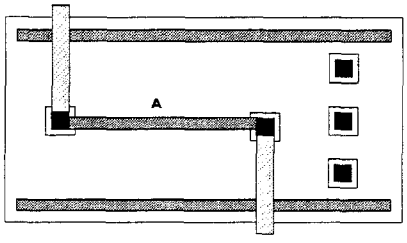


Figure 3b

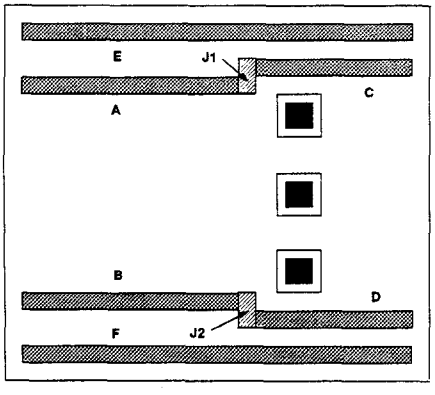


Figure 3c

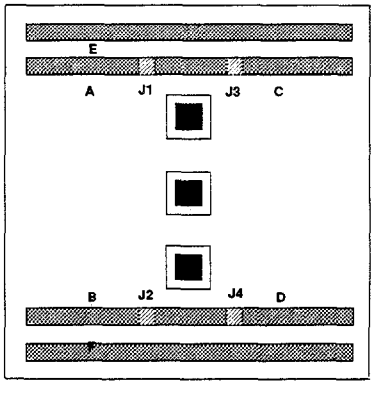


Figure 3d

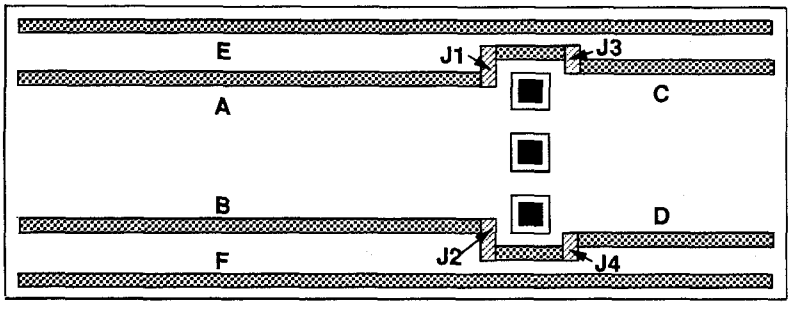


Figure 3e

Figure 3: Compacted layout examples which have different layout arrangement for WLM and yield.