NEW ROUTING AND COMPACTION STRATEGIES FOR YIELD ENHANCEMENT

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Abstract

Improvements in manufacturing lines alone can not compensate for the yield losses due to the increase in complexity of logic. Manufacturing yield improvement needs to be addressed during the physical layout synthesis stage itself. Several layout strategies for yield enhancement are proposed and they are illustrated with respect to channel compaction and routing in standard cell design. Algorithms and other implementation issues are discussed and examples illustrating these algorithms are presented.

1 Introduction

The importance of chip area minimization in increasing the manufacturing yield can not be over emphasized. Special CAD tools such as compactors are developed exclusively to perform area minimization. While the primary goal of all the compactors is to minimize the area, they include some secondary objectives like minimizing the total wire length, maximizing the utilization of a specific layer with better electrical characteristics, minimizing the number of vias, minimizing the number of jogs etc [7]. Most of these secondary objectives are oriented towards performance improvements.

Though the importance of yield enhancement is recognized [2, 8], so far very little attention was paid to it in physical layout synthesis. Compactors generate actual physical layouts which occupy minimum area either from symbolic layouts or from actual layouts generated by other layout synthesis tools [3, 10]. In constraint graph based compaction algorithms [7], physical connectivity and separation constraints between the elements are represented by a directed graph. The minimum achievable size of the layout is determined by the longest path (critical path) of the constrained graph. The elements on the critical path are placed at the minimum distances to minimize the area. Therefore, elements that lie on the critical path do not have freedom to move. However, elements that do not lie on the critical path can be placed in a variety of ways. So far this additional freedom has been utilized to optimize the performance such as wire length minimization. A new compaction algorithm is proposed in Section 2 to improve the yield of the compacted layout without increasing the area of the layout. The yield improvements achieved in two-layer routing channels by using this compaction algorithm are shown.

This new compaction algorithm improves the yield of the final design by distributing the spacing between non-critical elements so as to minimize the total number of faults that can occur in the design under particular manufacturing conditions, i.e., defect size distribution and defect densities for different failure types. In a similar way, further improvements in manufacturing yield can be achieved by modifying the widths of the non-critical elements.

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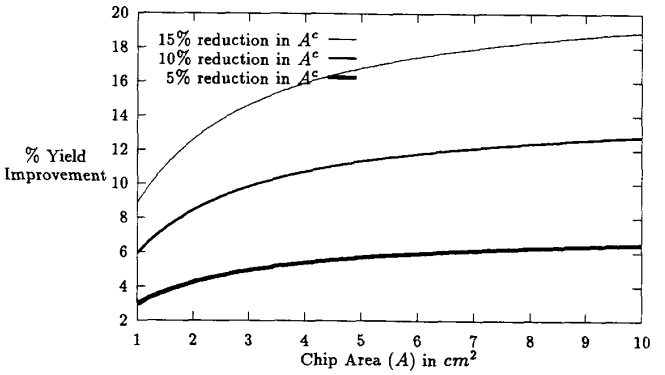

Figure 1: Effect of critical area reduction on yield improvement.

A new algorithm is proposed in Section 3 to optimize the width of the non-critical elements to enhance the yield.

Since compaction is the last stage of the layout synthesis, its effectiveness is highly dependent on the quality of the previous stages of the layout synthesis. For example, the quality of the routers will have a major impact on compaction. Therefore, improvements in the compaction stage alone can not drastically improve the yield. Several yield enhancement strategies for routing, layer assignment etc are proposed in Section 4. Conclusions are presented in Section 5.

2 Relocation of non-critical elements

After successful completion of channel routing, the channel height is minimized by compacting the channel in the vertical direction. Normally, compaction in the other direction is not possible due to positional constraints of the various elements of the cells. Yield enhancement can be achieved by minimizing the total critical area of open and short-circuit faults in the channel. The effect of reduction in critical area on the yield of a chip depends on its size. This is shown in Figure 1. In chips larger than 3 cm^2, yield improvements will be in the order of critical area reduction. For example, the yield of a 5 cm^2 chip can be improved by 11% with a 10% reduction in the critical area. (Yield is calculated using the three parameter negative binomial model with $Y_0 = 0.95$, $\alpha = 1.5$ and $\lambda = 1/cm^2$). This illustrates the significance of the critical area reduction in large area chips for yield enhancement.

Compactors place the elements as close as the design rules permit. Though this helps in minimizing the area, it unnecessarily packs many non-critical elements very close resulting in layers with large critical area of short-circuit faults. When relocating the wire segments,

the compactor may stretch them in order to maintain the original topology which results in longer nets and layers with large critical area of open-circuit faults. In the SPARCS compactor [3] this situation was improved by uniformly distributing the unused space among the non-critical elements. If we take the defect size distribution and the additional wire introduced in relocating the elements also into consideration, much better results from the yield's point of view can be obtained.

Since the defect size distribution is inversely proportional to the defect size raised to the power of 3 [11], change in the critical area will be nonuniform. For example, by increasing the spacing from 3 microns to 4 microns between the two wire segments of length 100 microns, the critical area of short-circuit faults can be reduced by 4 μm^2 whereas for the same amount of increase in spacing from 10 microns to 11 microns the corresponding reduction will be only 0.35 μm^2. Any increase in spacing beyond the largest defect size (about 20 microns) does not decrease the critical area at all. It is interesting to note that when changes are made in the layout to minimize the sensitivity of the design to one type of defects, the sensitivity to other defect types may increase. For example, when the width of the metal/active lines is increased to minimize the sensitivity of the design to open-circuit faults, its sensitivity to short-circuit faults and pinhole faults might increase. Therefore, critical area of open-circuit as well as short-circuit faults should be considered while finding an optimal location for non-critical elements.

2.1 Minimization of short-circuit type faults

The input to the algorithm is two directed graph representations of each layer of the compacted channel layout, one for horizontal wire segments and the other for the vertical wire segments (jogs). In the compacted layout all elements are placed at the minimum possible distances from the bottom of the layer. Each node in the graph represents a rectangular wire segment or a contact and each edge represents the spacing between two adjacent wire segments. The edge weight represents the distance between two adjacent wire segments and the node weight represents the average number of faults (λ). It depends on a) length and width of the wire segment, b) spacing between the wire segment and the wire segments above and c) spacing between the wire segment and the wire segments below. In addition, elements connected on both sides and their widths and spacings also influence the optimal location of an element. For example, in Figure 2a, element 18 is connected to two elements 17 and 19 which are above. When element 18 is moved up by one $LAMBDA$ (Λ) distance, the length of each jog will be reduced by one unit. This reduction in jog length will result in fewer open-circuit faults as well as short-circuit faults between adjacent jogs. On the other hand, if an element is connected to other elements which are below, its upward movement will result in extra jog lengths and the associated faults. For a wire segment, only elements in the same layer will be considered, where as for a contact, characteristics of the elements connected in the other layer also have to be considered.

First, node weights are calculated for all non-critical elements in the channel. Then, each non-critical element is searched in the breadth first order for an optimal location. Elements can be moved only in the upward direction since all the elements are at the minimum possible location to start with. If the current spacing between the node and each of its incident nodes is more than the minimum design rule specification, then that node can be

moved upwards. A wire segment is moved upwards by a minimum possible distance, i.e, by one Λ distance and the node weight is calculated. If the current node weight is smaller than the previous node weight, then the element is moved by another Λ distance. This procedure continues until the node weight in the new position is smaller than the previous one and the node position is updated. Then the next non-critical element will be processed.

Once all the non-critical elements are searched, the search will be repeated. The optimal location for an element can not be found in one iteration. This is due to the fact that the conditions under which an optimal location is found for an element may alter while processing its adjacent elements. It may take few iterations before final optimal positions are found for all the elements. For example, the optimal location for element 10 in Figure 2b is 11Λ from the top edge in the first iteration. The final optimal location for this element is 6Λ from the top edge and is found in the 5th iteration.

If an element can not be moved up any further due to minimum spacing constraints of any one of the elements above, then the element will be split into two elements and the graph is updated. Then the search will continue with the element that can be moved. Once all horizontal elements are processed, then vertical elements are processed in a similar manner.

2.2 Algorithm

```
1.Initialization
  {   Identify all non-critical elements in the graph and arrange them in BFS order;
      Initialize the node weights (nodewt-ref);
      term-flag = true;   }
2.Optimization
  while (term-flag)
  {   term-flag = false;
      for each non-critical element
      {   nodewt = nodewt-ref;
          new-nodewt = 0;
          while (new-nodewt < nodewt)
            if the element can be moved do
            {   move the element upward by 1 LAMBDA;
                calculate new-nodewt;
                if (new-nodewt < nodewt)
                {  update node positions
                   nodewt = new-nodewt;
                   new-nodewt = 0;
                   term-flag = true;   }   }
            else if the element can be split into two elements
            {  update the graph;
               initialize the nodewt of new node;     }   }   }
3. process the vertical jogs;
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The critical area of the wire segments is calculated using the analytical models reported in [11, 6]. The results of the layout optimization are shown in Figures 2(b) and 3. The

uncompacted layout of Figure 2 is a part of the layout generated by the router of MAGIC [9] layout editor from the netlist of *example3b* of [12]. The layout shown in Figure 2(a) is generated by the compactor PLOW [10] with automatic jog insertion, straightening and with minimum horizontal length of 12 Λ. The layout generated by our tool is shown in Figure 2(b). To characterize the impact of the layout optimization on manufacturing yield, the yield analysis tool LASER [5] is used. Defect size versus probability of failure plots are shown in Figure 3 both for short-circuit faults and open-circuit faults of metal-1 layer. The probability of a short-circuit type failure in metal-1 layer of the original compacted layout is 0.0118. This failure probability is reduced by 21% to 0.00932. Since the area and the total number of defects remain the same, the average number of faults is reduced by 21% due to this layout optimization. The reduction in probability of open-circuit faults is only 4% since the widths of the elements are not altered. This marginal decrease is due to reduction in jog lengths.

3 Wire width modifications

The compaction algorithm presented in the previous section for yield optimization is mainly based on optimal distribution of spacing among non-critical elements without increasing their widths. Therefore, most of the yield enhancement is due to reduction in short-circuit type faults. To achieve further yield enhancement, the effect of other types of faults should be minimized.

Layout synthesis tools such as routers are designed to generate layouts with minimum width elements to minimize the area. (Special layout requirements of power and ground and other critical signals may be met by manual layout or special tools). By increasing the width of some non-critical elements, open-circuit type faults can be minimized without any area penalties. These width changes do not affect the performance, since the RC characteristics of the interconnecting wires remain almost the same. However, similar changes on the active logic, clock and other long global nets require careful analysis of performance characteristics. The possible increase in the width depends on the length of the net and the electrical characteristics of the layer. A set of local rules were proposed in [1] for contacts, metal and polysilicon to enhance the yield. In this section we are proposing a general yield optimization methodology. The advantage of this method is that a layout can be optimized for given manufacturing conditions.

The width of the element will be increased in such a way that the total average number of faults λ is minimized. The optimal location for a non-critical element is calculated by minimizing the function given in equation 1.

$$\lambda(y) = A^c_{op}(y)D_0^{op} + A^c_{sh}(y)D_0^{sh} \tag{1}$$

where $\lambda(y)$ is the number of faults per unit area which can affect the functionality of the element, $A^c_{sh}(y)$ ($A^c_{op}(y)$) is the average critical area of short-circuit (open-circuit) faults, D_0^{sh} (D_0^{op}) is the defect density of short-circuit (open-circuit) faults and y represents the width and the location of the element.

3.1 Minimization of open-circuit type faults

Our yield optimization system accepts the graphical representation of the layout which is the same as the one described in Section 2. The defect size distribution $f(x)$, where x is the size of the defect, and the total number of defects D_0 (per unit area) for each defect type are the other inputs to the system. Each non-critical element is processed in a breadth first order. First, the optimal width increase at the top edge is found and then at the lower edge. The algorithm is similar to the one presented in Section 2 and is omitted for the sake of brevity. The significant difference is that the optimal widths for the elements will be found in one iteration.

The optimized layout shown in Figure 2(b) is processed using this algorithm and the results are shown in Figures 4 and 5. The layout shown in Figure 4(a) is optimized for a manufacturing environment where defect densities of both open- and short-circuit type are the same. Probability of failure versus defect size plots for both types of defects are shown in Figure 5. As expected, the probability of failure for short-circuit faults is increased by 7.4% and the probability for open-circuit faults is decreased by 21%. The overall decrease in the average number of faults is about 5% from the previous stage. The two stages of layout optimization for yield enhancement resulted in about 17% reduction in the number of faults in the metal-1 layer. Similar improvements are possible in the metal-2 layer as well. The same layout was optimized for conditions where the short-circuit type defect density is 10 times more than that of open-circuit type and it is shown in Figure 4(b). It is interesting to see the significant differences in the final layout under these two different manufacturing conditions.

4 Other layout strategies for yield enhancement

4.1 Layer assignment

In [8] three routing algorithms were used to generate a channel routing and the layouts were compared from the yield point of view. The results demonstrated the impact of the routing algorithms on yield. In two or multilayer channel routing, the majority of wire segments in a particular layer are either vertical or horizontal (HV, HVH etc). It is possible to minimize the critical area of short-circuit type faults by reassigning several horizontal wire segments to an otherwise vertical layer and vice versa whenever possible. This is very similar to maximizing the utilization of a preferred routing layer with better electrical characteristics achieved in routers by reassigning the wire segments, shifting or/and adding vias. All these strategies help us in minimizing the critical area of the short-circuit faults as well. However, the criteria for reassignment and adding vias for yield enhancement is different from that of a preferred layer maximization. For example, the number of additional vias worthwhile to add in converting a wire segment of one layer to a preferred layer is based on the length of the wire segment. This stems from the electrical characteristics of the wires involved and that of the vias (resistance and capacitance). Here we need to consider the overall reduction in the number of faults after modifications.

When a wire segment from a horizontal layer is moved to a vertical layer, reduction in critical area of short-circuit faults will be very likely because the wire segment will be moved from a dense region to a sparse region. There will be a change in the critical area of the open-circuit faults only if there is a change in the width of the wire segments (minimum width design rules) or change in the wire length. It is to be noted that layer reassignment for yield enhancement and maximization of the preferred layer may work against each other depending on the technology. In such design situations the trade-off between these two parameters must be chosen carefully.

4.2 Via and wire length minimization

Most of the existing CAD tools try to minimize the total number of vias in the design. Since the minimum width and spacing requirements for vias are larger than the lines, generally more compact designs are possible with fewer vias. Sometimes, just to avoid a via, routers may introduce very long wires in the nets as long as these wires are not a part of the longest net. This certainly results in layers with higher critical areas. On the contrary, in certain situations it may be worthwhile to introduce some vias (or leave some vias intact) to avoid unnecessary additional wiring. Analogous to minimum wire length requirements for introducing additional vias in the preferred layer maximization problem, we should introduce some criteria to remove/add a via in terms of wire length/critical area.

4.3 Uniform distribution of the unused area among various modules

We discussed so far the efficient management of free space within a given module without paying much attention to the overall chip layout. CAD tools of different design stages generate the modules within the smallest possible area. There are however, design situations where we need not pursue this goal in every module so rigorously. For example, in an ASIC chip where area is I/O bound, the empty space between pads and active area can be utilized to enhance the yield of the chip without any performance degradation. In such a design situation, channels may be rerouted with more emphasis on the yield considerations. Requirements of packaging (aspect ratio), performance based design requirements, differences in shapes and sizes of various modules are some of the sources of these unused area.

5 Conclusions

Two yield enhancement algorithms have been presented in this paper. In Section 2, a new algorithm is proposed for layout compactors to minimize the average number of short-circuit type faults in the layout. In Section 3, a yield enhancement technique is presented to minimize the open-circuit type faults. When these two techniques are applied, overall faults of these two types will be minimized. These two yield enhancement techniques have been implemented and this tool can be integarted into any physical layout synthesis system with minor changes to the existing algorithms. It is shown that upto 20% reduction in open- and short-circuit faults can be achieved in one layer. Even in layouts generated by very good tools, there will be scope for yield improvement. Further improvements are posssible by incorporating the yield enhancement criteria for other defect types. We intend to extend this work by incorporating contact and pinhole and other defect types. The yield

enhancement techniques discussed in Section 4 may be implemented either in routers or in compactors. Further analysis needs to be done on implementation aspects.

The most significant aspect of the yield enhancement techniques proposed in this paper is that no additional area is required. The yield enhancements can be realized almost free except for marginal increase in computational time of the CAD tools. Another important aspect is that a layout can be optimized for given manufacturing conditions. We have illustrated some of the yield enhancement techniques with respect to channel routing and compaction. We intend to extend these yield enhancement techniques for other design styles and layouts, e.g., gate matrix designs, multilayer channel routing, general cell channel routing etc.

Acknowledgements: This work was supported in part by IBM under contract 81775. The authors would like to thank Dr. Jose Pineda de Gyvez for providing the yield analysis software.

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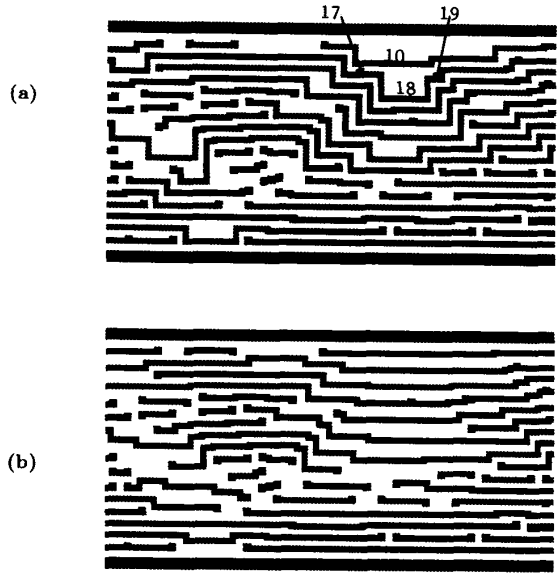
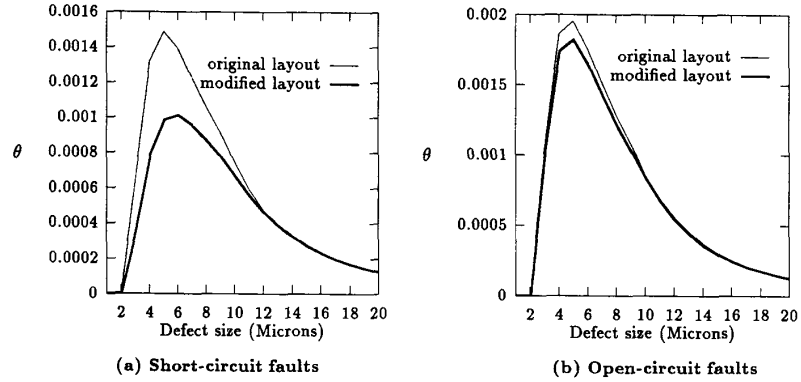


Figure 2: Minimization of short-circuit type faults
(a): Original layout (b): Modified layout



(a) Short-circuit faults **(b) Open-circuit faults**

Figure 3: Probability of failure vs. Defect size.

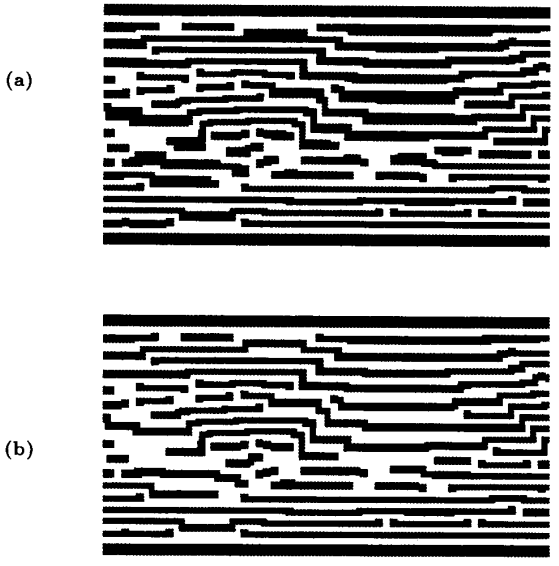
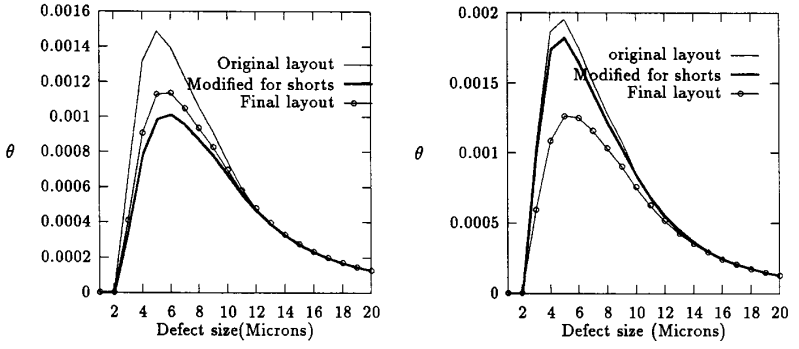


Figure 4: Minimization of open-circuit type faults
(a): Modified for same defect density
(b): Modified for higher short-circuit defect density



(a) Short-circuit faults **(b) Open-circuit faults**

Figure 5: Probability of failure vs. Defect size.