Best Paper Award

THE IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING Best Paper Award is presented to the authors of that paper considered by the Transactions' Editorial Staff and reviewers to be the outstanding paper published during the year. The Award is based on the accuracy, originality, and importance of the technical concept, as well as the quality and readability of the manuscript. The Best Paper is also based on the immediate or potential impact that this work will have on the overall semiconductor manufacturing industry.

The IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING Best Paper Award, presented at the annual Advanced Semiconductor Manufacturing Conference and Workshop, recognizes the on-going partnership of this conference and the IEEE.

The Editorial Staff is pleased to announce that the paper entitled "Layout Synthesis Techniques for Yield Enhancement," by V. K. R. Chiluvuri and I. Koren has been recognized as the best paper published in the 1995 TRANSACTIONS. This paper, which appeared in the May issue, has been chosen because it represents a novel method to apply yield enhancement techniques at a high level of design abstraction. The techniques discussed enable the IC to be desensitized to point defect related yield loss without increasing the die area during the layout synthesis phase of IC development. The techniques described in this paper have been used in a commercially available CAD framework.

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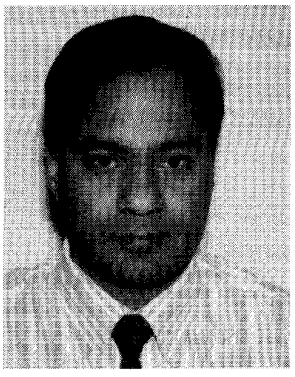

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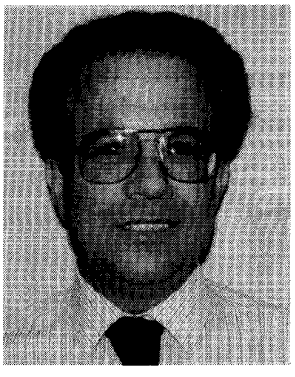
He is currently a Senior Staff Engineer at Motorola, Austin, TX. From 1984 to 1990, he was with Wipro Information Technology Ltd., Bangalore, India. From 1993 to 1994, he worked at the IBM T. J. Watson Research Center, Yorktown Heights, NY. His research interests include layout synthesis, CAD for yield and manufacturability, and VLSI design.



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His current research interests are fault-tolerant architectures, models for yield and performance, floor-planning of VLSI chips, and computer arithmetic. He published extensively in several IEEE TRANSACTIONS and has over 100 publications in refereed journals and conferences. He was a Co-Guest Editor for the IEEE TRANSACTIONS ON COMPUTERS special issue on high-yield VLSI systems, April 1989. Since January 1992, he has served on the editorial board of this TRANSACTIONS. He also served as Program Committee Member for numerous conferences. He is the General Chair of the 1996 IEEE Symposium on Defect and Fault Tolerance in VLSI Systems (DFT96), Boston, MA, November 1996, and the General Chair of the 1996 Conference on Parallel Architectures and Compilation Techniques (PACT96), Boston, MA, October 1996. He has edited and co-authored the book *Defect and Fault-Tolerance in VLSI Systems,* Vol. 1, 1989, (New York: Plenum). He is the author of the textbook, *Computer Arithmetic Algorithms,* Prentice-Hall, 1993.