# Reliability analysis of hybrid redundancy systems

I. Koren, D.Sc., Mem.I.E.E.E., and E. Shalev, M.Sc.

*Indexing terms:* *Reliability, Switches and switching theory, Hybrid redundancy, Threshold voters*

**Abstract:** The paper presents a new approach to the reliability evaluation of redundant systems. The exact logic design of the switches is analysed in order to distinguish between fatal and nonfatal faults in the switching logic. System unreliability is then calculated by summing the probabilities that unrecoverable faults occur. In addition to the more accurate reliability evaluation achieved by the new approach, it is also useful for comparing various designs of the switching logic or different switching strategies.

## 1 Introduction

Hybrid redundancy is a well known technique for reliability enhancement [1–6]. It effectively increases the reliability of a module by replicating it $m$ times and selecting a correct output using a voting scheme. The voting is performed only on a core of $N$ modules ($N < m$), while the rest of the modules serve as spares. A hybrid redundancy system provides means for detecting faulty modules and includes a switching logic for selecting a core of $N$ properly operating modules out of the $m$ modules. A minimal core of $N = 3$ modules (TMR core) produces a correct output as long as at least two modules function properly.

A relatively simple design of a switching network for a hybrid system has been presented in Reference 1 using iterative cells, as shown in Fig. 1. The iterative cells determine

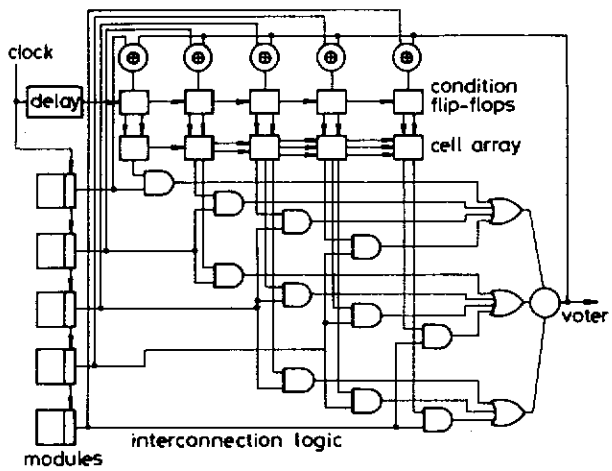


**Fig. 1** *Hybrid system (TMR core and two spares) with an iterative cell switch*

the first $N$ nonfailed modules and assign them to be voted on. Each cell receives the number of functional modules that are already connected to the voter, through the $y_0$, $y_1$ and $y_2$ outputs of the preceding cell (Fig. 2), and compares it to the core size $N$. If the count is smaller than $N$ the cell connects its module to the voter and sends to its successor the (three-bit) code word corresponding to the increased count. However, if its module is faulty (indicated by $c_i = 0$, Fig. 2) the cell does not connect its module, and the count is not increased.

A module may include any number of output lines, denoted by $z_1$ to $z_n$. A hybrid system assembled of such modules includes $n$ voters; each one votes on a set of outputs $z_i$. Hence, the voter and interconnection gates shown in Fig. 1 are replicated $n$ times. Each XOR gate in Fig. 1 is replaced by $n$ XOR gates, all ORed together so that a fault in any output sets the condition FF. The condition FF itself and the iterative cells are not replicated.

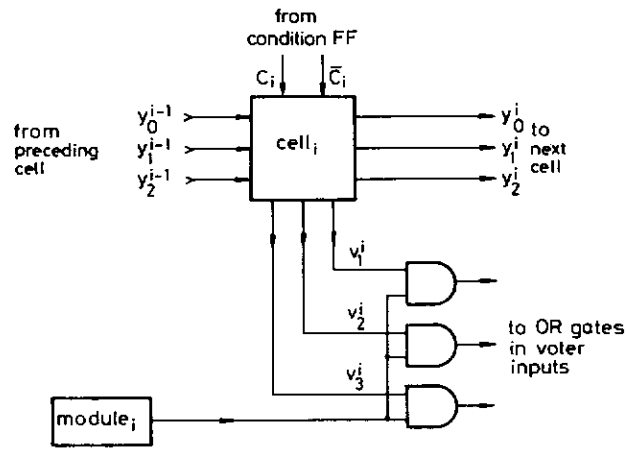


**Fig. 2** *Iterative cell*

## 2 Reliability of hybrid systems

The reliability of hybrid systems has been evaluated until now by multiplying the reliability of the system obtained when perfect switches are assumed with the reliability of the switches [2, 3]. As noted in Reference 2, this simplified modelling underestimates system reliability since it assumes that each single fault in the switching network is fatal. In practice, many switching faults are tolerable. If, for example, a condition FF fails, and it wrongly indicates a fault in its module, then the module is disconnected and replaced by a spare, allowing the system to recover. Similarly, many of the switching faults do not necessarily cause a system failure unless they are accompanied by some additional faults.

In the following we evaluate the reliability of a hybrid system, using a detailed examination of the faults. Only fatal combinations of faults in the switches and modules are assumed to affect reliability.

We adopt the 'gate level of modelling' [2] which assumes that every gate has an independent exponential reliability function. The exact logic structure of the switches determines their effect on the system reliability. Consequently, we have to deal with each gate separately. For such a gate we assume that its output may fail either as stuck at 0 or stuck at 1 with equal probabilities. We denote by $\mu$ the failure rate of each gate.

In contrast, the exact design of the module is not considered, since general conclusions appropriate to various types of modules have to be derived. Hence, we assign the module a total failure rate $\lambda$, and we restrict our attention

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The authors are with the Department of Electrical Engineering, Technion–Israel Institute of Technology, Haifa 32000, Israel

to the output signals. We assume that when a module fails, it produces output signals which are the worst for the system operation. Thus, a conservative evaluation of the reliability is obtained. Our assumption is clearly justified when modules are retried to distinguish between transient and permanent faults [1, 7], since there is a high probability that at least one of the retries will yield the worst-case output signal.

In what follows we refer only to the practical mission-time range where the system reliability is above 0.9. Such a mission time is in most cases considerably shorter than the mean lifetime of a module ($1/\lambda$). We also assume that complex modules such as microprocessors are used (consisting of 10,000 gates and over). For such mission times and module complexity, the unreliability of the switches (about 50 gates each) is low compared to that of the modules. Hence, the effect of a single-gate fault in the switching network on the system unreliability is greater than that of a multiple-gate fault which has a lower probability of occurrence. Therefore, multiple faults in the switching logic are ignored in the analysis.

The unreliability of the system is calculated by summing the probabilities of fatal faults, i.e. faults that result in a system failure. We partition these faults into three subsets; namely switching faults, voting faults and module faults.

### 2.1 Fatal switching faults

In this subset we include combinations of a fault in the switching logic and a limited number of module faults which by themselves would not cause a system failure. Fatal module faults are included in the third subset. To ensure that all possible switching faults are considered, the following three steps are taken:

(i) listing the functions of the switch

(ii) assuming an error in each of the above functions and listing the possible functional faults

(iii) analysis of the switch design to identify the gates where each of the above faults may be originated, note that a fault-simulation program can be employed for this purpose (e.g. [6])

Step (i): A switch performs the following functions:

(*a*) determines whether the module it controls has to serve as a spare module or a core module; this is accomplished by counting the properly functioning modules

(*b*) monitors the status of the module (faulty or functional)

(*c*) selects the voter input (if any) to which the module should be connected

(*d*) connects the module to the voter through the interconnection gates

Step (ii): The possible faults in the above listed functions are further partitioned into three groups:

group *a*: disconnection faults which prevent one or more functional modules from being connected to the voter

group *b*: faults which cause an undesirable connection, according to the following:

a faulty module is connected to the voter
a module is connected to two voter inputs
a spare module is connected to the voter

group *c*: faults in the interconnection gates, which cause a voter input to be stuck at an incorrect logical level

Step (iii): in this step each of the above faults is analysed to identify their possible sources; in this process we restrict our attention to faults caused by a single gate failure in the switches and any number of module faults. Although only single physical failures in the switches are considered, more than one of the faults of step (ii) may occur simultaneously since some of the iterative cell gates are involved in more than one of the switching functions (e.g. connecting the module and producing the count).

The exact reliability expressions are quite lengthy; hence, we introduce here in detail only the calculation of the disconnection faults which are the most dominant switching faults. For the other faults we present approximate expressions which refer only to events including a minimum number of faults in the modules. The complete derivations appear in Reference 8.

Next, we present the switching faults included in groups *a*, *b* and *c*, and we derive expressions for their probabilities.

*2.1.1 Group a switching faults—disconnection faults:* According to the iterative cell realisation, shown in Fig. 3, the connection of each module to the voter depends

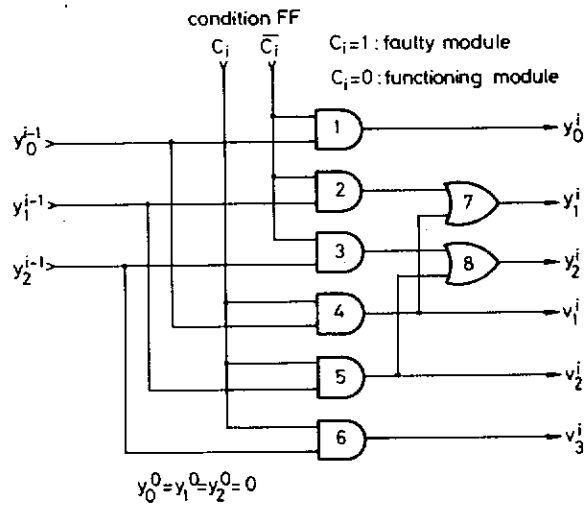


**Fig. 3** *Iterative cell realisation*

on a three-bit code which is passed along the cells. Only one of these three bits may be set at any time, thus indicating to which one of the three voter inputs (if any) the cell may connect its module. Any fault in an iterative cell which incorrectly resets this bit results in an all-zero code, which indicates erroneously that all three voter inputs are already connected. This code word causes the cell to disconnect its module and send the same code word to its successor, resulting in disconnection of all succeeding modules. Other faults which may disconnect a functional module can occur in the XOR gates or the condition FF connected to the cell, but, since these faults affect only one module, their effect on system reliability is substantially smaller than that of the faults in the iterative cell, and they can be neglected.

A list of all disconnection faults appears in Table 1. In this table $n_1$, $n_2$ and $n_3$ denote the serial numbers of the three first operational modules ($1 \leqslant n_i \leqslant m$; $i = 1, 2, 3$).

**Table 1: Disconnection faults**

| Fault in switch $j$ | Module status | Faulty gate (Fig. 3) | Modules connected to voter |
|---|---|---|---|
| $j < n_1$ | faulty | 1 | 0 |
| $j = n_1$ | operational | 4 or 7 or 9 | <2 |
| $n_2 > j > n_1$ | faulty | 2 or 7 | 1 |
| $j = n_2$ | operational | 5 or 9 | 1 |
| $j = n_2$ | operational | 8 | 2 |
| $n_3 > j > n_2$ | faulty | 3 or 8 | 2 |
| $j = n_3$ | operational | 6 or 9 | 2 |

The index of the faulty switch $j$ assumes all the possible values (see first column of Table 1) when $n_1$, $n_2$ and $n_3$ scan the values from 1 to $m$. Consequently, Table 1 includes all the possible disconnection faults.

The first four faults leave the system with less than two modules connected to the voter and, consequently, the system fails. In the other three cases two modules are still connected, and the system may continue to function but without being able to tolerate any fault in these modules.

The probability of a system failure due to disconnection faults is calculated by adding seven unreliability terms, one for each of the rows of Table 1. The first four terms are computed in a combinatorial manner, since the order of events does not matter. In contrast, the last three terms have to be calculated using integrals since they describe events where the system arrives first at the state described in the Table, and then an additional module fails. In these three cases, the same faults occurring in a different order will still allow the system to function properly. The seven unreliability terms corresponding to the rows in Table 1, and appearing in the same order, are presented in eqn. 1:

$$
\begin{aligned}
P_{DISCONNECT} = {} & 0.5 \sum_{n_1=2}^{m-1} (1 - e^{-\lambda T})^{n_1 - 1} \\
& \times e^{-\lambda T}(1 - e^{-(n_1-1)\mu T}) \\
& + 0.5 \sum_{n_1=1}^{m-1} (1 - e^{-\lambda T})^{n_1 - 1} \\
& \times e^{-\lambda T}(1 - e^{-3\mu T}) \\
& + 0.5 \sum_{n_2=3}^{m} \sum_{n_1=1}^{n_2-2} (1 - e^{-\lambda T})^{n_2 - 2} \\
& \times e^{-2\lambda T}(1 - e^{-(n_2-n_1-1)2\mu T}) \\
& + 0.5 \sum_{n_2=2}^{m} (n_2 - 1)(1 - e^{-\lambda T})^{n_2 - 2} \\
& \times e^{-2\lambda T}(1 - e^{-2\mu T}) \\
& + 0.5 \sum_{n_3=3}^{m} \int_0^T \binom{n_3 - 1}{2} (1 - e^{-\lambda \tau})^{n_3 - 3} \\
& \times e^{-3\lambda \tau}(1 - e^{-\mu \tau}) 2\lambda \, d\tau \\
& + 0.5 \sum_{n_3=4}^{m} \sum_{n_2=2}^{n_3-2} (n_2 - 1) \int_0^T (1 - e^{-\lambda \tau})^{n_3 - 3} \\
& \times e^{-3\lambda \tau}(1 - e^{-2(n_3-n_2-1)\mu \tau}) 2\lambda \, d\tau \\
& + 0.5 \sum_{n_3=3}^{m} \int_0^T \binom{n_3 - 1}{2} (1 - e^{-\lambda \tau})^{n_3 - 3} \\
& \times e^{-3\lambda \tau}(1 - e^{-2\mu \tau}) 2\lambda \, d\tau \qquad (1)
\end{aligned}
$$

To clarify eqn. 1, the first and the last terms are explained, as they represent a combinatorial term and an integral term, respectively.

The first term (related to the first row of Table 1) is associated with a fault in switch $j$, $1 \leqslant j < n_1$, where $n_1$ varies between 2 and $m - 1$. We restrict the calculation to $n_1 \leqslant m - 1$ to ensure that at least two functional modules are left in the system. The case where $n_1 = m$ is a fatal module fault and will, therefore, be included in the third subset of faults.

The summand is the probability that all the first $n_1 - 1$ modules fail (since $n_1$ is the number of the first operational module), module $n_1$ itself does not fail, and one of the first $n_1 - 1$ switches fails. The 0.5 factor multiplying this term, as well as the other terms, represents the conditional probability of a $s$-$a$-0 fault in the switch.

The last term in eqn. 1 corresponds to the last row of Table 1 and includes a summation over all possible values for $n_3$, which is the number of the third operational module, whose switch is assumed to fail. The integral in this term is the probability that the following sequence of faults occurs:

(i) First, $n_3 - 3$ modules out of the $n_3 - 1$ modules which precede module $n_3$ fail, thus causing module $n_3$ to become the third functioning module.

(ii) Next, a fault occurs in the switch of module $n_3$, leaving the system with only two functioning modules connected to the voter. According to Table 1, two gates may be involved in this fault, with total failure rate of $2\mu$.

(iii) At last, one of the two modules which are connected to the voter fails, resulting in a system failure.

*2.1.2 Group b switching faults:* This group includes all the faults causing undesirable connections. The first is the connection of a failed module to the voter. Such a fault may occur when the fault detection section of the switch malfunctions. This section includes the XOR gate and condition FF (Fig. 1). Gates 4, 5 or 6 in the switch (Fig. 3) can also cause such a connection fault. This fault is not fatal when it occurs by itself. However, when it is followed by a fault in an additional core module, a majority of incorrect signals at the voter inputs is formed, and the system fails.

The probability that this sequence of faults happens is

$$
\begin{aligned}
P_{CONNECTION} = {} & \int_0^T \text{Prob.}\left\{\begin{array}{c}\text{a core module and its detector} \\ \text{fail during time period } [0, \tau]\end{array}\right\} \\
& \times \text{Prob.}\left\{\begin{array}{c}\text{one of two core modules} \\ \text{fails at instant } \tau\end{array}\right\} \\
& + \int_0^T \text{Prob.}\left\{\begin{array}{c}\text{any module and one of its associated gates} \\ \text{(4, 5, 6) fail during time period } [0, \tau]\end{array}\right\} \\
& \times \text{Prob.}\left\{\begin{array}{c}\text{one of two core modules which are} \\ \text{connected to unaffected voter inputs fails}\end{array}\right\}
\end{aligned}
$$

The first integral calculates the probability that the fault detection section of the switch will fail. A fault in this section affects the system only when occurring in the switch of a core module. The second integral refers to a $s$-$a$-1 fault that occurs in gates 4 or 5 or 6 (Fig. 3) of any switch, resulting in the connection of the corresponding module to the voter, regardless of the module condition.

The fault-detection section of a switch includes a XOR gate for each of the $n$ output lines of the module, an OR gate that ORs the outputs of these XOR gates and a FF with an estimated complexity of ten gates. In total it includes approximately $n + 11$ gates. Substituting into eqn. 2 yields

$$
\begin{aligned}
P_{CONNECTION} = {} & 0.5 \int_0^T 3(1 - e^{-\lambda \tau}) \\
& \times e^{-2\lambda \tau}[1 - e^{-(11+n)\mu \tau}] 2\lambda \, d\tau \\
& + 0.5 \int_0^T m(1 - e^{-\lambda \tau}) \\
& \times e^{-2\lambda \tau}[1 - e^{-3\mu \tau}] 2\lambda \, d\tau \qquad (3)
\end{aligned}
$$

A second fault in group $b$ is a double connection of a module. Normally only one of the signals $v_1$ to $v_3$ (Fig. 2) is activated (logic 1), but a $s$-$a$-1 fault in gates 4–6 (Fig. 3) may activate an additional signal. This will cause the connection of the corresponding module to two voter inputs. If, following this fault, the module fails, two of the three voter inputs become incorrect and the system fails. The probability of such an event is

$$P_{DOUBLE} = \int_0^T \text{Prob.}\left\{\begin{array}{c}\text{second connection of a}\\ \text{core module during } [0, \tau]\end{array}\right\} \times \text{Prob.}\left\{\begin{array}{c}\text{the doubly connected module}\\ \text{fails at instant } \tau\end{array}\right\}$$
$$= 8\int_0^T \frac{1}{2}(1 - e^{-2\mu\tau})e^{-\lambda\tau}\lambda\, d\tau \qquad (4)$$

The factor 8 is the number of possible faults, including the case where a fault in gate 4 or 5 introduces an error in the code which is passed along the cells, resulting in a simultaneous double connection of two modules.

The third fault in group $b$ is the connection of a spare module to the voter. As long as this spare module is functional its connection has no effect on the system. The system may be affected by such a fault if this module fails and the system cannot disconnect it due to some previous faults. Since a large number of faults must be involved here before the system fails, its effect on system reliability has been shown to be negligible [8].

*2.1.3 Group c switching faults:* A fault occurring at one of the $3n$ OR gates connected to the voter inputs, or a $s$-$a$-1 fault at any of the $3nm$ interconnection gates, leaves the voter with only two correct inputs. If a module connected to one of these two inputs fails, the system fails. The total number of gates which are involved in the failure is $3(m + 1)n$ for a system of $m$ modules and $n$ outputs. The probability of such a failure is

$$P_{STUCK} = \int_0^T \text{Prob.}\left\{\begin{array}{c}\text{an OR gate fails or an interconnection}\\ \text{gate becomes } s\text{-}a\text{-}1 \text{ during } [0, \tau]\end{array}\right\} \times \text{Prob.}\left\{\begin{array}{c}\text{one of the modules connected}\\ \text{to the remaining}\\ \text{voter inputs, fails at instant } \tau\end{array}\right\}$$
$$= \int_0^T (1 - e^{-3(m+1)n\mu\tau})e^{-2\lambda\tau}2\lambda\, d\tau \qquad (5)$$

## 2.2 Fatal voter faults

In addition to the fatal switching faults there exist fatal voter faults and fatal module faults. The system uses $n$ voters, one per a system output, and any fault that affects a voter output causes a system failure. We assume an AND/OR realisation of the three-input voter as shown in Fig. 4. A $s$-$a$-1 fault in any one of the four gates, or a $s$-$a$-0 fault in gate 4, affects the output of the voter. A $s$-$a$-0 fault in one of the AND gates is fatal only when followed by a false-0 signal in another gate input due to a module fault. The unreliability term corresponding to these faults is

$$P_{VOTERS} = \text{Prob.}\left\{\begin{array}{c}\text{a } s\text{-}a\text{-}1 \text{ fault at}\\ \text{any gate}\end{array}\right\} + \text{Prob.}\left\{\begin{array}{c}\text{a } s\text{-}a\text{-}0 \text{ fault at the}\\ \text{OR gate}\end{array}\right\} + \int_0^T \text{Prob.}\left\{\begin{array}{c}\text{a } s\text{-}a\text{-}0 \text{ at the AND}\\ \text{gate during } [0, \tau]\end{array}\right\} \times \text{Prob.}\left\{\begin{array}{c}\text{a module which is connected to the two functioning}\\ \text{AND gates, produces a false 0 at instant } \tau\end{array}\right\}$$
$$= 0.5(1 - e^{-4n\mu T}) + 0.5(1 - e^{-n\mu T}) + 0.5\int_0^T (1 - e^{-3n\mu\tau})e^{-\lambda\tau}\lambda\, d\tau \qquad (6)$$

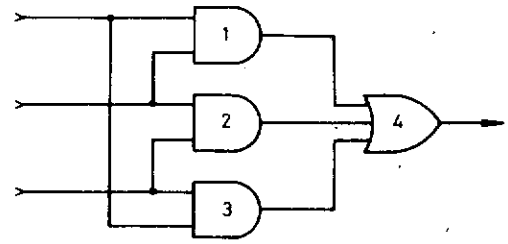


**Fig. 4** *Three-input voter*

## 2.3 Fatal module faults

When no fatal faults occur in the switches or voters, the system may fail due to faults in more than $m$-2 modules (out of $m$), with probability [3]

$$P_{MOD} = \text{Prob.}\{\text{failure due to module faults}\} = (1 - R)^m + mR(1 - R)^{m-1} \qquad (7)$$

where $R = e^{-\lambda T}$ is the reliability of a single module.

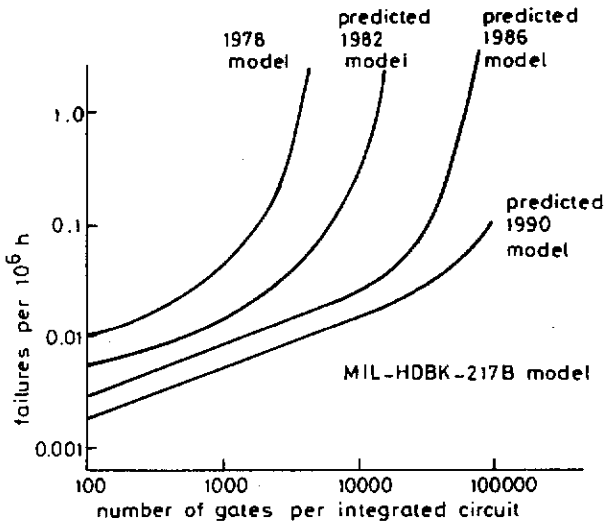


**Fig. 5** *IC failure rate against gate count*

## 2.4 Total unreliability calculation

The total unreliability of the hybrid system is obtained by summing the probabilities of all fatal faults. For a numerical evaluation of the unreliability, the ratio between the failure rates in the switches and modules has to be specified. This ratio depends on the complexity of the module integrated circuits and the switch integrated circuits. The dependence of the failure rate of an IC, on its complexity in the present technology and its predicted values are shown in Fig. 5[9].

We consider for example modules made of 20 000 gates each, having $n = 8$ outputs. Each module is assumed to consist of 4 ICs (e.g. a CPU, ROM, RAM and I/O port). The switching logic and voters can be included in two ICs, about 200 gates each. The ratio between the failure rates of a module IC and a switch IC according to Fig. 5 is about ten in the 1982 model and about five in later models. The switching faults (eqns. 1–5) have a greater effect compared to module faults; as this ratio is decreasing, we will use, therefore, the latter ratio of 5 to check the worst-case behaviour of the system. The resulting ratio between $\lambda$, the failure rate of the 4 ICs module, and $\mu$, the failure rate of a single gate in the switching logic, is 4000.

The unreliability of the hybrid system with a varying number of modules is depicted in Fig. 6 and compared to

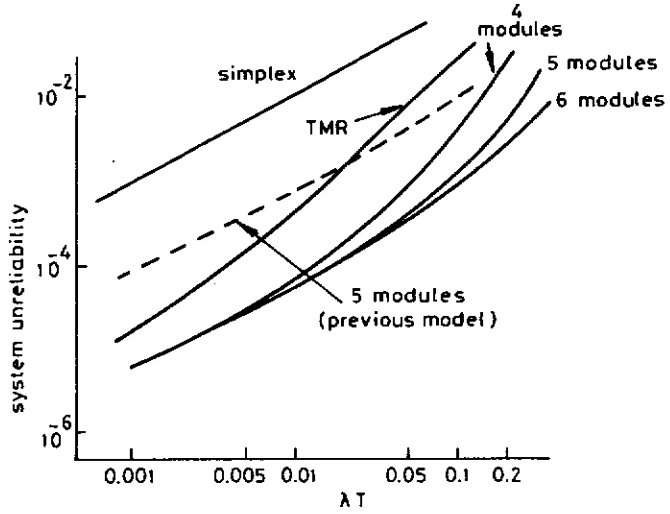


**Fig. 6** *Unreliability of a multiple output hybrid system*

the unreliability of a simplex system (with no redundancy) and of a TMR system. The latter includes the unreliability of the voters. Fig. 6 shows that the hybrid system is more reliable than the other two systems for a wide range of mission times. A system having five modules is preferable to a system with four modules, for mission times longer than about 0.01 of the mean lifetime of a module. Adding a sixth module improves the reliability significantly only for mission times longer than about 0.1 of the mean lifetime.

According to these results, the performance of a hybrid system is substantially better than what is expected when using the previous model [2] which assumes that all the switching faults are fatal. When compared to the previous model shown by the dotted line in Fig. 6 (with the same value of the ratio $\lambda/\mu$), the new model shows a lower unreliability (with a factor of up to 13.5) and a wider range of mission times where the hybrid system is more reliable than TMR.

## 3 Other voter configurations

The total unreliability of the system above has been calculated by summing the various unreliability components. These components are shown, in Fig. 7, divided into three major categories of failure causes: modules, voters and switches. The voters' unreliability is the dominant component in a large range of mission times, and, therefore, it must be reduced if one wishes to improve the system reliability. It is possible in certain applications to use the technique of voter redundancy to reduce the effect of voter faults on the system reliability [5]. For example, the microcomputer system shown in Fig. 8 uses voters to select a correct set of output signals out of the $m$ memory modules. These voters also play an important role in synchronising the microprocessors [10]. The voter

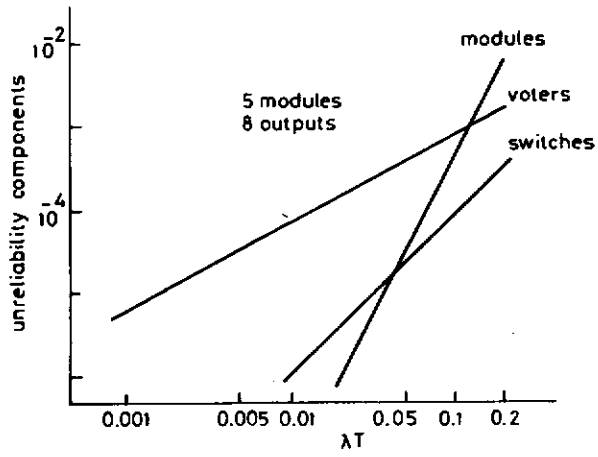


**Fig. 7** *Components of the unreliability*

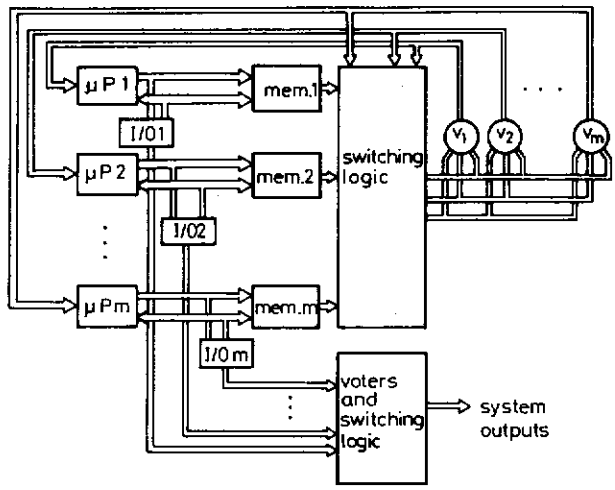


**Fig. 8** *Microcomputer hybrid system*

redundancy prevents the system from failing due to a single faulty voter, since each voter affects only one microprocessor. Thus, the voters' unreliability component shown in Fig. 7 is greatly reduced. Still, the nonredundant voters in the I/O section of Fig. 8 have a critical effect on the system outputs. The reliability calculation of such a system has been presented in Reference 11.

### 3.1 Hybrid systems with threshold voters

Most of the interconnection gates in the hybrid system can be eliminated, by replacing each three-input majority voter with a voter having a dedicated input for each module and acting as a threshold voter [1, 2]. The output of a threshold voter is 1 only when the number of logic 1 input signals equals or exceeds a given threshold. By using a threshold of two, the threshold voter performs the same function as the majority voter. Only one AND gate is used to control the connection of each output of a module to the voter. A faulty or a spare module can be inhibited, by using this gate, from passing a logic 1 signal to the voter.

The price paid for simplifying the interconnection logic is the greater complexity of the voter. With AND/OR realisation of the voters, a five-input threshold voter includes almost three times as many gates as a majority voter with three inputs. Since the reliability of the voter gates has a greater effect on system reliability than the

interconnection gates, replacing the majority voters with threshold voters may decrease system reliability. Note that this is true while assuming the same failure rates in the switches and the voters. If more reliable components are selected for the voter, then the threshold voter may be preferable.

## 4 Conclusions

A new approach to the reliability analysis of redundant fault-tolerant systems has been presented. The approach is based on the investigation of the signal paths inside the switches and yields more accurate results than previous methods.

This approach has been used to analyse hybrid redundancy systems with majority voters, yielding a system reliability that is much higher than was previously calculated. The difference between the results of the new and previous models is particularly important when analysing a system which includes many output lines, and thus a more complicated switching network. In this case the over simplified approach of the previous model may lead to the conclusion that the hybrid technique is less reliable than simpler techniques such as TMR.

In addition to evaluating system reliability, the new approach provides separate unreliability terms for each type of the various switching faults. This information can be used to identify the dominant faults and to change the switch design in order to improve reliability.

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