

$$d_{2k} = \lfloor d_k/2 \rfloor \quad (9)$$

$$d_{2k+1} = (2^n - 1) - d_{2k} \quad (10)$$

for $k = 0, 1, \dots, 2^{n-1} - 1$; where $\lfloor x \rfloor$ is the "floor" function denoting the greatest integer smaller than x .

Proof: The recursive formulas will be proved separately.

$$1) d_{2k} = \lfloor d_k/2 \rfloor:$$

Let the binary representation of k be (4). Then

$$(2k)_2 = (k_n k_{n-1} \dots k_2 k_1 0) \quad (11)$$

The inverse Gray codes of the bit-reverses of $(k)_2$ and $(2k)_2$ are, respectively,

$$(d_k)_2 = (x_1 x_2 \dots x_{n-1} x_n) \quad (12)$$

and

$$(d_{2k})_2 = (0 y_2 y_3 \dots y_{n-1} y_n) \quad (13)$$

where

$$x_i = \sum_{j=1}^i k_j \quad (14)$$

and

$$y_i = 0 \oplus \sum_{j=1}^{i-1} k_j = x_{i-1}, \quad i = 2, \dots, n-1. \quad (15)$$

That is $(d_{2k})_2$ is obtained from $(d_k)_2$ by shifting the bits of the latter one bit to the right. Hence $d_{2k} = \lfloor d_k/2 \rfloor$.

$$2) d_{2k+1} = (2^n - 1) - d_{2k}:$$

From (11) we can write immediately

$$(2k+1)_2 = (k_n k_{n-1} \dots k_2 k_1 1). \quad (16)$$

Let

$$(d_{2k+1})_2 = (1 z_2 z_3 \dots z_{n-1} z_n). \quad (17)$$

From (5), (6), and (16),

$$z_i = 1 \oplus \sum_{j=1}^{i-1} k_j = \bar{x}_{i-1} = \bar{y}_i, \quad i = 2, \dots, n-1. \quad (18)$$

Since $(d_{2k+1})_2$ is the one's complement of $(d_{2k})_2$ it follows that $(d_{2k+1} + d_{2k})_2 = (11 \dots 11)$, and hence the result.

In order to generate the 2^n elements of \bar{S}_n the algorithm based on (8), (9), and (10) requires 2^n computation steps. This is approximately half the

$$\sum_{i=0}^{n-1} 2^{n-i} = 2(2^n - 1)$$

computation steps required by the algorithm in [1]. The total number of operations necessary for binary implementation of the proposed algorithm are one assignment, $2^{n-1} - 1$ one-bit right shifts, and 2^{n-1} subtractions, whereas the previous algorithm requires $2^n - 1$ assignments (indexing operations) and $2^n - 1$ subtractions. Even if the cost of an assignment operation is neglected, the present algorithm is superior since a one-bit right shift is simpler than subtraction. Though the time complexities of both algorithms are of the order of 2^n , the proposed algorithm is easier to implement since it is not recursive with respect to n .

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Analysis of the Signal Reliability Measure and an Evaluation Procedure

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Abstract—The classical reliability measure of digital circuits, known as functional reliability, assumes that the circuit fails whenever a fault is present in it. It has long been known that this reliability measure is overly pessimistic since digital circuits may produce correct output signals even when some faults are present in them. A different reliability measure, known as signal reliability, is the probability that the circuit output is correct. This reliability measure is analyzed first and compared to the functional reliability measure. Next, a new procedure for the evaluation of the signal reliability measure is presented.

Index Terms—Combinational circuits, functional reliability, probability of fault occurrence, signal probability, signal reliability.

I. INTRODUCTION

The reliability of digital circuits can be evaluated using two different measures. The first measure is called *functional reliability* and is the probability that the circuit realizes the desired design function. The second measure is called *signal reliability* and is the probability that the circuit output is correct.

The functional reliability measure assumes that the circuit fails whenever a fault is present in it. It has long been known that this reliability measure is exceedingly pessimistic since digital circuits may produce correct output signals even when some faults are present in them [1]–[5]. Moreover, this measure is too simplified; when evaluating the reliability of a circuit we consider only the number of basic elements which may fail (number of leads if lead failures are considered or number of gates if gate failures are considered), while the exact structure of the circuit is not taken into account. The more accurate signal reliability measure is analyzed in Section II and is compared to the functional reliability measure.

Two different approaches to the evaluations of the signal reliability of general combinational circuits were presented by Ogus [2]. The first method requires the evaluation of the behavior of each possible fault in the circuit. In the second method a special fault circuit is formed and faults are injected into it through special control input lines. Although the second method is more efficient than the first one it is still impractical because of the amount of computation involved. An improved method for evaluation of the signal reliability measure in combinational circuits is presented in Section IV. This method evaluates the signal reliability in a recursive way and can easily be automated.

II. RELIABILITY MEASURES

The reliability of a logical circuit depends upon the possible faults and their probabilities of occurrence. The probability of a fault, denoted by s , is usually assumed to be time dependent and the time function $s(t) = 1 - e^{-at}$ where a is the failure rate, is used frequently. Thus at $t = 0$ the probability of the fault is $s(0) = 0$ and it increases with t . Consequently, the reliability of the circuit is time dependent. This reliability can be evaluated using two different reliability measures, the functional reliability, denoted by $FR(t)$, and the signal reliability, denoted by $SR(t)$. These reliabilities are defined as follows:

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$$FR(t) = \Pr \{ \text{the circuit is fault-free at time } t \}$$

$$SR(t) = \Pr \{ \text{the output signal is correct at time } t \}.$$

Since logical circuits may produce correct output signals even when some faults are present in them, we have

$$SR(t) \geq FR(t) \quad \text{for all } t.$$

One of the most important applications of reliability analysis is the prediction of mission time, i.e., the time the circuit will operate at or above a given reliability. In order to predict the mission time we need the accumulative reliability in the time interval $[0, t]$ rather than at the instant t . Hence, we define the accumulative functional reliability and the accumulative signal reliability, denoted by $R_F(t)$ and $R_S(t)$, respectively, as follows.

$$R_F(t)$$

$$= \Pr \{ \text{the circuit is fault-free in the time interval } [0, t] \}$$

$$R_S(t)$$

$$= \Pr \{ \text{the output signals are correct in the time interval } [0, t] \}.$$

It is clear that

$$R_S(t) \geq R_F(t).$$

If only permanent faults are considered and no repair is taking place, then clearly $R_F(t) = FR(t)$ for all t . The nonaccumulative signal reliability $SR(t)$ and the accumulative signal reliability $R_S(t)$ are not necessarily equal since the output signal may be incorrect at time instant t_1 and correct at a later time instant t_2 ($t_2 > t_1$) depending upon the input signals applied to the circuit. Consequently

$$SR(t) \geq R_S(t) \geq R_F(t) = FR(t), \quad \text{for all } t. \quad (1)$$

Thus, $SR(t)$ and $R_F(t)$ are the upper and lower bounds, respectively, of the accumulative signal reliability. The fact that $R_S(t) \geq R_F(t)$ implies that the functional lifetime (the time to failure) and the signal lifetime (the time to the first incorrect output signal) of the circuit, denoted by T_F and T_S , respectively, satisfy $T_S \geq T_F$. The problem of evaluating the difference $T_S - T_F$ was studied by Sheddletsky and McCluskey [7], [8]. They have shown that the number of time units in this difference is equal to the error latency of the circuit where the error latency of a circuit is defined as the number of input vectors applied to the circuit having a fault until the first incorrect output signal due to that fault is observed.

In this work we restrict ourselves to evaluation of the nonaccumulative signal reliability rather than the more complex accumulative signal reliability for which we have no efficient evaluation methods at this moment. For convenience, the nonaccumulative signal reliability will be called signal reliability. In the following we indicate possible applications of the signal reliability in addition to those mentioned in [2], [3], [6], and [9]. Besides being the upper bound of $R_S(t)$, the signal reliability $SR(t)$ is useful if the circuit is not used continuously and we are interested in predicting the probability that it will operate correctly at some time t in the future (or at some specific instants t_1, t_2, \dots) while the operation of the circuit until that time is of no concern.

Another application of the signal reliability is to compare between different realizations of a logical circuit. Employing the functional reliability measure results in a less accurate reliability comparison of different designs of a digital circuit. When the functional reliability is evaluated, the reliability of the basic element of the circuit is raised to the number of these basic elements in the circuit, where the basic element is a lead if lead failures are considered or a gate if gate failures are considered, e.g., [5], [10]. Although reliability is a function of the complexity of the circuit,

the complexity may not be treated as a simple function of the number of basic elements, as was already indicated by Ingle and Siewiorek [10]. Contrary to the functional reliability measure, the signal reliability of a circuit depends upon the exact structure of the circuit, the nature of the possible failures and their probabilities of occurrence, thus yielding a more accurate reliability comparison of different designs.

In the next sections we present a procedure for the evaluation of the signal reliability of combinational circuits. For convenience, we shall omit t as an argument of the reliability and failure probability functions and these functions will be understood to be time dependent.

III. BASIC DEFINITIONS AND ASSUMPTIONS

The signal reliability of a circuit depends upon the possible failures and their probabilities of occurrence. We assume that the possible failures are multiple lead failures of the stuck-at type, i.e., any line X in the circuit may be stuck at one (abbreviated s-a-1) or stuck at zero (s-a-0).

Let s_X denote the probability of occurrence of a single fault on line X . This fault can be either an s-a-0 fault with probability q_{0X} , or an s-a-1 fault with probability q_{1X} , satisfying

$$s_X = q_{0X} + q_{1X}.$$

The signal reliability of line X , designated $R(X)$, is defined as the probability that the logic signal on line X is correct. Since the correct logic signal on line X can be either 0 or 1 we define the 0(1) signal reliability as follows [2]:

$$R_0(X) = \Pr \{ \text{line } X \text{ is correctly a 0} \}$$

$$R_1(X) = \Pr \{ \text{line } X \text{ is correctly a 1} \}.$$

Clearly

$$R(X) = R_0(X) + R_1(X). \quad (2)$$

Similarly, we define the signal unreliability, denoted $Q(X)$, and the 0(1) signal unreliability [2]

$$Q(X) = \Pr \{ \text{the logic signal on line } X \text{ is incorrect} \}$$

$$Q_0(X) = \Pr \{ \text{line } X \text{ is incorrectly a 0} \}$$

$$Q_1(X) = \Pr \{ \text{line } X \text{ is incorrectly a 1} \}.$$

Clearly

$$Q(X) = Q_0(X) + Q_1(X)$$

and

$$R(X) + Q(X) = 1. \quad (3)$$

According to the method proposed here, the signal reliabilities and unreliabilities of the lines in the circuit are evaluated recursively, i.e., the values of R_0 , R_1 , Q_0 , and Q_1 for the output line of every subcircuit are calculated using the values of these reliability functions for its input lines. In order to simplify the equations relating the output and input signal reliabilities and unreliabilities of a subcircuit, we establish a simple model for the circuit. In this model we insert in each line of the circuit a special subnetwork called Fault Occurrence Network (FON). Only in these special subnetworks may s-a-0 or s-a-1 faults occur, while the other parts of the circuit, i.e., the subcircuits and the primary input lines, are fault free. For example, the appropriate model for a NAND gate is shown in Fig. 1.

The proposed model enables us to derive separately two sets of equations. The first set relates the output and input signal reliabilities and unreliabilities of an FON in a single line. The second set

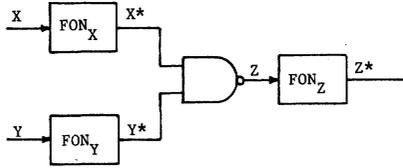


Fig. 1. The model for a NAND gate.

of equations relates the output and input signal reliabilities of a subcircuit which is fault free according to our model.

We derive now the first set of equations for a single line. Let X^* denote the output line of an FON whose input line is X , and suppose that the values of $R_1(X)$, $R_0(X)$, $Q_1(X)$, and $Q_0(X)$ are given, thus

$$\begin{aligned} R_1(X^*) &= \Pr \{X^* \text{ is correctly a } 1\} \\ &= \Pr \{X \text{ is correctly a } 1 \cap \text{no fault occurred}\} \\ &\quad + \Pr \{(X \text{ is correctly a } 1 \text{ or incorrectly a } 0) \\ &\quad \cap (\text{an } s\text{-a-1 fault occurred})\}. \end{aligned}$$

Since the occurrence of a fault in this line is independent of the correctness of the signal X , we obtain

$$R_1(X^*) = R_1(X) \cdot (1 - s_x) + [R_1(X) + Q_0(X)]q_{1x}.$$

Simple algebraic manipulations yield

$$R_1(X^*) = R_1(X) \cdot (1 - q_{0x}) + Q_0(X) \cdot q_{1x}. \quad (4)$$

In a similar manner we can prove the following equations:

$$R_0(X^*) = R_0(X) \cdot (1 - q_{1x}) + Q_1(X) \cdot q_{0x} \quad (5)$$

$$Q_1(X^*) = Q_1(X) \cdot (1 - q_{0x}) + R_0(X) \cdot q_{1x} \quad (6)$$

$$Q_0(X^*) = Q_0(X) \cdot (1 - q_{1x}) + R_1(X) \cdot q_{0x}. \quad (7)$$

If line X is a primary input line to the circuit, it is according to our assumptions fault free, hence

$$\begin{aligned} Q_0(X) &= Q_1(X) = 0 \\ R_1(X) &= \Pr \{X = 1\}; R_0(X) = \Pr \{X = 0\}. \end{aligned} \quad (8)$$

The last two probabilities, denoted p_x and $1 - p_x$, respectively, were called signal probabilities and were studied by Parker and McCluskey [4], [6]. These signal probabilities can be calculated for each line in the circuit, using the signal reliabilities and unreliabilities, as follows:

$$p_x = \Pr \{X = 1\} = R_1(X) + Q_1(X) \quad (9)$$

$$1 - p_x = \Pr \{X = 0\} = R_0(X) + Q_0(X). \quad (10)$$

IV. SIGNAL RELIABILITY OF COMBINATIONAL CIRCUITS

Most combinational circuits are constructed out of basic gates like AND, OR, NAND, NOR, and NOT. We will derive now, for these basic gates, a single set of equations for calculating the output signal reliability. Each of these basic gates can be uniquely described by a binary vector [11]. Let X_1, X_2, \dots, X_n denote the input lines of a gate, and let Y denote the output line. This gate is described by the vector $(\alpha_1, \alpha_2, \dots, \alpha_n, \beta)$, where $\alpha_1, \alpha_2, \dots, \alpha_n$ is the only input combination for which the output equals β . For example, a three-input NOR gate is described by the vector (0001) since the gate output equals 1 only for the input combination (000) and equals 0 for any other input combination.

The equations for calculating the output signal reliabilities and unreliabilities of a basic gate are given in the following theorem.

Theorem 4.1: The output signal reliabilities and unreliabilities of an n -input basic gate, whose input signals X_1, X_2, \dots, X_n are independent, are given by the following equations:

$$R_\beta(Y) = \prod_{i=1}^n R_{\alpha_i}(X_i) \quad (11)$$

$$Q_\beta(Y) = \prod_{i=1}^n [Q_{\alpha_i}(X_i) + R_{\alpha_i}(X_i)] - R_\beta(Y) \quad (12)$$

$$Q_{\bar{\beta}}(Y) = \prod_{i=1}^n [Q_{\bar{\alpha}_i}(X_i) + R_{\bar{\alpha}_i}(X_i)] - R_\beta(Y) \quad (13)$$

$$R_{\bar{\beta}}(Y) = 1 - [R_\beta(Y) + Q_\beta(Y) + Q_{\bar{\beta}}(Y)] \quad (14)$$

where $\alpha_1 \alpha_2 \dots \alpha_n \beta$ is the binary vector describing this gate.

Proof: According to our model the gate is fault free, therefore

$$\begin{aligned} R_\beta(Y) &= \Pr \{Y \text{ is correctly a } \beta\} \\ &= \Pr \{\text{each } X_i \text{ is correctly a } \alpha_i\}. \end{aligned}$$

The n input signals are independent, hence

$$= \prod_{i=1}^n \Pr \{X_i \text{ is correctly a } \alpha_i\} = \prod_{i=1}^n R_{\alpha_i}(X_i).$$

To prove (12) note that

$$\begin{aligned} R_\beta(Y) + Q_\beta(Y) &= \Pr \{Y \text{ is correctly or incorrectly a } \beta\} \\ &= \Pr \{\text{each } X_i \text{ is correctly or incorrectly an } \alpha_i\}. \end{aligned}$$

The independence between the input signals results in

$$= \prod_{i=1}^n [R_{\alpha_i}(X_i) + Q_{\alpha_i}(X_i)]$$

and (12) follows.

In a similar manner we prove (13):

$$\begin{aligned} R_\beta(Y) + Q_{\bar{\beta}}(Y) &= \Pr \{Y \text{ is correctly a } \beta \text{ or incorrectly a } \bar{\beta}\} \\ &= \Pr \{Y \text{ is correctly a } \beta \text{ or should be a } \beta\} \\ &= \Pr \{\text{each } X_i \text{ is correctly an } \alpha_i \text{ or should be } \alpha_i\} \\ &= \prod_{i=1}^n [R_{\alpha_i}(X_i) + Q_{\bar{\alpha}_i}(X_i)]. \end{aligned}$$

Since $R_\beta(Y) + R_{\bar{\beta}}(Y) + Q_\beta(Y) + Q_{\bar{\beta}}(Y) = 1$, (14) follows. Q.E.D.

Equations (11)–(14) can be employed for signal reliability calculations in any fan-out-free circuit since the assumed independence of all primary input lines implies independence of the input signals to each gate. The main problem in extending these equations to general combinational circuits is the existence of reconverging fan-out lines causing dependencies between gate input signals. A similar problem concerning signal probabilities was studied by Parker and McCluskey [6]. They presented the following equations for the case where the signals are independent, e.g., primary input signals

$$\Pr \{\bar{A} = 1\} = 1 - \Pr \{A = 1\} \quad (16)$$

$$\Pr \{AB = 1\} = \Pr \{A = 1\} \cdot \Pr \{B = 1\} \quad (17)$$

$$\begin{aligned} \Pr \{A \vee B = 1\} &= \Pr \{A = 1\} + \Pr \{B = 1\} \\ &\quad - \Pr \{A = 1\} \cdot \Pr \{B = 1\}. \end{aligned} \quad (18)$$

It was suggested in [6] that these equations can be used in the case where the signals are dependent by suppressing the resulting ex-

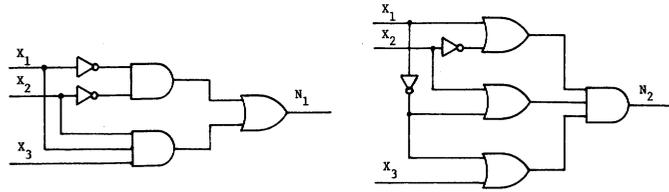


Fig. 2. Two realizations of the function $f(X_1, X_2, X_3) = \sum (0, 1, 7)$.

ponents of the signal probabilities. We shall now state and prove formally the above.

Theorem 4.2: The output signal probability of a basic gate whose input signals are dependent can be computed by using (16)–(18) and suppressing the resulting exponents of the fan-out signals' probabilities.

Proof: See Appendix A.

In the following theorem we show that the principle of exponent suppression can be used in signal reliability calculations as well.

Theorem 4.3: The output signal reliabilities and unreliabilities of a basic gate whose input signals are dependent can be calculated using (11)–(14) and suppressing the exponents of the fan-out signals' reliabilities and unreliabilities.

Proof: Using the method suggested by Ogus [2] we can form for every circuit with output signal Z a new circuit with output signal H satisfying

$$\Pr \{H = 1\} = \Pr \{Z \text{ is correctly a } 1\} = R_1(Z).$$

In a similar way we can form circuits satisfying $\Pr \{H = 1\} = R_0(Z)$, or $\Pr \{H = 1\} = Q_1(Z)$, or $\Pr \{H = 1\} = Q_0(Z)$. According to Theorem 4.2, the probability $\Pr \{H = 1\}$ can be calculated using the principle of exponent suppression. Consequently, this principle can be employed in signal reliability and unreliability calculations as well. Q.E.D.

The following two examples illustrate the calculation of signal reliabilities of general combinational circuits.

Example: The Boolean function $f(X_1, X_2, X_3) = \sum (0, 1, 7)$ can be realized in two different ways as shown in Fig. 2. The first is a sum-of-products realization

$$N_1 = \bar{X}_1 \bar{X}_2 + X_1 X_2 X_3.$$

The second is a product-of-sums realization

$$N_2 = (X_1 + \bar{X}_2)(\bar{X}_1 + X_2)(\bar{X}_1 + X_3).$$

The output signal reliabilities of these two circuits were computed using an APL program. In these computations we assumed that all possible faults are equally likely, i.e., $q_0 = q_1 = s/2$ for all lines and that

$$P\{X_1 = 1\} = P\{X_2 = 1\} = P\{X_3 = 1\} = 0.5,$$

i.e., all input combinations are equally likely. The results are plotted in Fig. 3(a) as a function of the fault probability s and in Fig. 3(b) as a function of time. In Fig. 3(b) the exponential function for the fault probability (i.e., $s(t) = 1 - e^{-at}$) is used and the time has been normalized; one time unit is equal to the mean lifetime $1/a$. The main conclusion that can be drawn from this example is that a circuit having a larger number of gates and lines and consequently a larger number of possible faults, is not necessarily less reliable, e.g., in the example the circuit N_2 has a larger number of gates and lines, however $R(N_2) > R(N_1)$ for $s > 0.145$, or equivalently, for $t > (1/a)0.156$. When comparing the reliability of these two circuits using the functional reliability measure, the

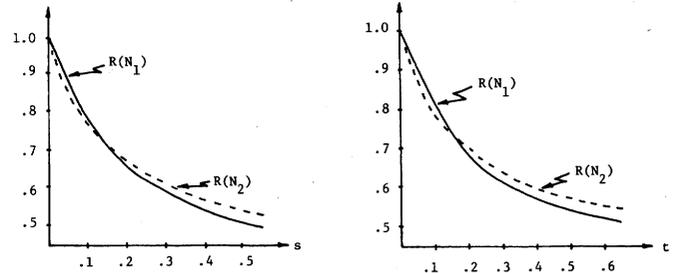


Fig. 3. The signal reliabilities of the circuits in Fig. 2.

circuit N_1 having a smaller number of possible faults is assumed to be more reliable than N_2 for any t .

Another application of signal reliability calculations is to evaluate the increase or decrease in reliability, caused by using TMR configurations, as shown in the following example.

Example: A binary full-adder (FA) is realized in a TMR configuration as shown in Fig. 4. The signal reliabilities of the lines A_1, C_1, A , and C were computed assuming that the probabilities of all possible faults are equal and that all input combinations are equally likely. The results are plotted in Fig. 5 as a function of the fault probability s . From this graph we can see that the usage of a TMR configuration will increase the signal reliability of both output lines only for $0 < s < 0.11$, or equivalently, for $0 < t < (1/a)0.1165$. A similar comparison using the functional reliability measure results in a more pessimistic conclusion that the reliability of the TMR configuration is greater than the reliability of the FA module only for $0 < s < 0.029$, or equivalently, for $0 < t < (1/a)0.0294$.

V. CONCLUSIONS

Two different forms of the signal reliability measure, the accumulative and the nonaccumulative signal reliability, have been defined.

These two forms were analyzed and compared to the known functional reliability measure. A recursive procedure for calculating the nonaccumulative signal reliability has been developed. This procedure simplifies the computations involved in evaluating the signal reliability.

APPENDIX A

Proof of Theorem 4.2: We prove the theorem for an AND gate with input signals A and B and output signal C . The proofs for other kinds of gates are similar and will therefore be omitted.

Dependency between the input signals A and B is caused only by reconverging fan-out lines [6] in the subnetwork feeding A and B . We assume that X_1, X_2, \dots, X_n are the primary input lines of the circuit and that X_1, X_2, \dots, X_k , ($k \leq n$), are the only fan-out lines reconverging at this AND gate. This assumption is justified as follows: Every Boolean function can be realized by a circuit in which all fan-out lines are primary input lines, and since every Boolean function has a unique probability expression [6], our

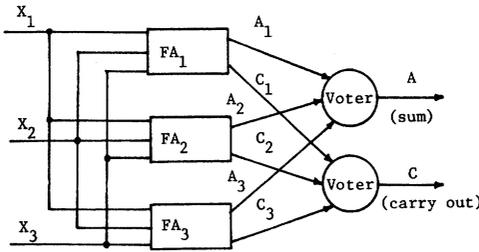


Fig. 4. A TMR configuration of a full-adder.

assumption is justified. Consequently, we obtain

$$A = F(X_1, X_2, \dots, X_k, X_{k+1}, \dots, X_m), \quad (m \leq n)$$

$$B = G(X_1, X_2, \dots, X_k, X_{m+1}, \dots, X_n)$$

where the three sets (X_1, X_2, \dots, X_k) , (X_{k+1}, \dots, X_m) , and (X_{m+1}, \dots, X_n) are disjoint.

Both functions F and G can be described in a canonical sum of products form. Summing up all products containing the same minterm of (X_1, \dots, X_k) yields

$$A = \bigcup_{i=0}^{2^k-1} F_i(X_{k+1}, \dots, X_m) \cdot m_i(X_1, \dots, X_k) \quad (A.1)$$

$$B = \bigcup_{j=0}^{2^k-1} G_j(X_{m+1}, \dots, X_n) \cdot m_j(X_1, \dots, X_k) \quad (A.2)$$

where $m_i(X_1, \dots, X_k)$, $i = 0, 1, \dots, 2^k - 1$ is the i th minterm.

No two products in the expression for A can be simultaneously 1, hence the signal probability of A is [6]

$$\begin{aligned} p_A &= \Pr \{A = 1\} \\ &= \sum_{i=0}^{2^k-1} \Pr \{F_i(X_{k+1}, \dots, X_m) \cdot m_i(X_1, \dots, X_k) = 1\}. \end{aligned}$$

The terms F_i and m_i are independent, therefore

$$p_A = \sum_{i=0}^{2^k-1} p_{F_i} p_{m_i} \quad (A.3)$$

where

$$p_{F_i} = \Pr \{F_i(X_{k+1}, \dots, X_m) = 1\}$$

and

$$p_{m_i} = \Pr \{m_i(X_1, \dots, X_k) = 1\}.$$

In a similar way we obtain

$$p_B = \sum_{j=0}^{2^k-1} p_{G_j} p_{m_j} \quad (A.4)$$

where p_{G_j} is defined similarly to p_{F_i} .

In order to obtain a logical expression for the output line C we perform an AND operation on (A.1) and (A.2). Since the AND operation of $m_i(X_1, \dots, X_k)$ and $m_j(X_1, \dots, X_k)$ equals 0 if $i \neq j$, we obtain

$$C = AB = \bigcup_{i=0}^{2^k-1} F_i(X_{k+1}, \dots, X_m) \cdot G_i(X_{m+1}, \dots, X_n) m_i(X_1, \dots, X_k).$$

Using the same reasoning as for A , the signal probability of C is given by

$$p_C = \sum_{i=0}^{2^k-1} p_{F_i} p_{G_i} p_{m_i}. \quad (A.5)$$

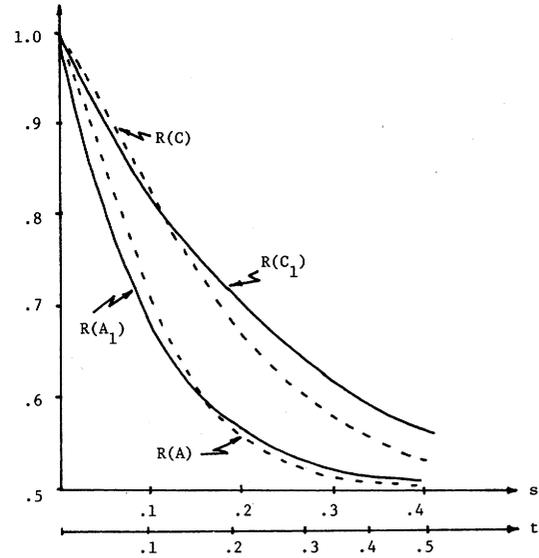


Fig. 5. The signal reliabilities of the TMR configuration in Fig. 4.

We will now use (17) to derive an expression for the signal probability of C and show that it is equal to (A.5) if the resulting exponents are suppressed. Substituting (A.3) and (A.4) into (17) yields

$$p_A p_B = \left(\sum_{i=0}^{2^k-1} p_{F_i} p_{m_i} \right) \left(\sum_{j=0}^{2^k-1} p_{G_j} p_{m_j} \right). \quad (A.6)$$

We prove now that if exponents are suppressed, the products $p_{m_i} p_{m_j}$ satisfy

$$p_{m_i} p_{m_j} = \begin{cases} p_{m_i}, & \text{if } i = j \\ 0, & \text{otherwise.} \end{cases} \quad (A.7)$$

In the logical expression for the minterm m_i , each of the input variables X_1, \dots, X_k appears in its complemented or uncomplemented form, hence

$$m_i(X_1, \dots, X_k) = \bigcap_{l=1}^k \tilde{X}_l, \quad \text{where } \tilde{X}_l = X_l \text{ or } \bar{X}_l.$$

Since the input variables are independent, we obtain

$$p_{m_i} = \prod_{l=1}^k \Pr \{\tilde{X}_l = 1\}$$

where

$$\Pr \{\tilde{X}_l = 1\} = \begin{cases} p_{X_l} & \text{if } \tilde{X}_l = X_l \\ 1 - p_{X_l} & \text{if } \tilde{X}_l = \bar{X}_l. \end{cases}$$

If $i = j$ the product $p_{m_i} p_{m_j}$ equals

$$p_{m_i}^2 = \prod_{l=1}^k (\Pr \{\tilde{X}_l = 1\})^2$$

where

$$(\Pr \{\tilde{X}_l = 1\})^2 = \begin{cases} p_{X_l}^2, & \text{if } \tilde{X}_l = X_l \\ 1 - 2p_{X_l} + p_{X_l}^2, & \text{if } \tilde{X}_l = \bar{X}_l. \end{cases}$$

Using the principle of exponent suppression we obtain

$$(\Pr \{\tilde{X}_l = 1\})^2 = \begin{cases} p_{X_l} & \text{if } \tilde{X}_l = X_l \\ 1 - p_{X_l} & \text{if } \tilde{X}_l = \bar{X}_l \end{cases} = \Pr \{\tilde{X}_l = 1\}.$$

Consequently

$$p_{m_i}^2 = p_{m_i}.$$

If $i \neq j$ there is at least one variable $X_a \in \{X_1, X_2, \dots, X_k\}$ which appears in its uncomplemented form in $m_i(m_j)$ and in its complemented form in $m_j(m_i)$, hence

$$P_{m_i P_{m_j}} = P \cdot p_{X_a}(1 - p_{X_a})$$

where P is a product of probabilities not including p_{X_a} .

Using the principle of exponent suppression, we obtain

$$P(p_{X_a} - p_{X_a}^2) = P(p_{X_a} - p_{X_a}) = 0.$$

The proof of (A.7) is now complete. Substituting (A.7) in (A.6) yields

$$P_A P_B = \sum_{i=0}^{2k-1} P_{F_i} P_{G_i} P_{m_i} = P_C.$$

Q.E.D.

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Aspects of the Upper Bounds of Finite Input-Memory and Finite Output-Memory Sequential Machines

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Abstract—In this paper upper bounds on the finite input-memory μ_i and finite output-memory μ_o of n -state completely specified sequential machines (CSSM's) and incompletely specified sequential machines (ISSM's) are investigated. It is observed through computational means that $N = n(n - 1)/2$ is not a tight upper bound for finite input-memory of ISSM's and finite output-memory of both CSSM's and ISSM's. Tight upper bounds of $\mu_i, \mu_o \leq 14$ for 6-state machines

and tight upper bounds of $\mu_i, \mu_o \leq 20$ for 7-state machines are obtained.

Index Terms—Completely specified machine, finite input-memory, finite output-memory, incompletely specified machine, sequential machine, upper bound.

INTRODUCTION

The study of finite memory sequential machines was initiated by Zadeh and Simon [9]. Gill [2] proved that for reduced n -state CSSM's finite memory $\mu \leq N$ where $N = n(n - 1)/2$, finite input-memory $\mu_i \leq n - 1$, and finite output-memory $\mu_o \leq N$. Later, Gill [5] showed that the upper bound for finite memory of reduced n -state CSSM's was tight for an N -ary-input and binary-output. Massey [6] improved this result by showing for every n there exists a ternary-input-binary-output n -state CSSM with finite memory $\mu = N$. He conjectured that this result could not be extended to binary-input-binary-output n -state CSSM's for $n \geq 6$. Newborn [7] disproved this conjecture and later [8] showed that the upper bound for finite memory was achievable for n -state binary-input-binary-output CSSM's. Kambayashi *et al.* [4] independently arrived at the same result and started an investigation into the tightness of the upper bound of finite output-memory machines [5]. They showed that for every n there exist binary-input-ternary-output n -state CSSM's with $\mu_o = N$. They constructed binary-input-binary-output n -state CSSM's with $\mu_o = N$ for $n < 6$ and left $n \geq 6$ as an open question.

Recently, Toke and Vairavan [11] have shown that the upper bound for μ_o is $O(n^2)$ for n -state machines. Toke [10] has also gotten tight upper bounds on the output-memory of certain classes of n -state machines.

This paper resolves the open problem of whether N is a tight upper bound for finite output-memory and gives tight upper bounds for the finite input-memory of 6-state and 7-state ISSM's and tight upper bounds for the finite output-memory of 6-state and 7-state CSSM's and ISSM's. The approach taken is computational in nature—theorems are proved to reduce the set of machines that could possess maximum finite output-(input-) memory and this set is enumerated and checked with a backtracking procedure. A similar technique has been used in the solution of the four-color problem [1].

PRELIMINARIES

A sequential machine M is defined by a finite state set S , a finite input set I , a finite output set O ,

$$\delta: S \times I \rightarrow S \text{ next-state function,}$$

and

$$\lambda: S \times I \rightarrow O \text{ output function.}$$

In this paper only binary-input-binary-output (BIBO) sequential machines will be considered. An incompletely specified sequential machine (ISSM) is one where at least one of the functions δ, λ is partial. A sequential machine is said to be *nondegenerate* if δ is an onto function. The sequel will be concerned with BIBO nondegenerate CSSM's and ISSM's.

An input sequence $i_1 i_2 \dots i_k$ is said to be *applicable* to a machine M if there exist two states s, s' such that

$$s' = \delta(\delta(\dots \delta(\delta(s, i_1), i_2) \dots, i_{k-1}), i_k).$$

An output sequence $0_1 0_2 \dots 0_k$ is said to be *generated* by a machine M if there exists a state s and an input sequence $i_1 i_2 \dots i_k$ such that

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