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SIGNAL RELIABILITY OF COMBINATIONAL AND SEQUENTIAL CIRCUITS

Israel Koren
Department of Electrical Engineering and Computer Science
University of California
Santa Barbara, CA 93106

A new measure of logic circuit reliability, called signal reliability, was introduced by Ogus.[1] The signal reliability of a circuit is defined as the probability that the circuit output is correct, assuming that multiple faults of the stuck-at type may occur. Two different approaches to the evaluation of the signal reliability were presented by Ogus. However, both procedures are restricted to combinational circuits.

In this paper we extend this new reliability measure to sequential circuits. We present a new method for evaluation of signal reliability which can be applied to sequential as well as combinational circuits.

I. Introduction

Logical circuits may produce correct output signals even when some faults are present in them. Given the nature and probabilities of the possible faults in the circuit we can determine the probability of the output being correct for any input combination. This probability was introduced by Ogus as a new measure of logic circuit reliability, called signal reliability.[1]

Two different approaches to the evaluation of the signal reliability of general combinational circuits were presented by Ogus.[1] The first one is straightforward but is impractical because of the amount of computation involved. The second method is based upon the probabilistic model of combinational circuits which was introduced by Parker and McCluskey.[2,3] The latter method is more efficient than the first one; however, it is also restricted to combinational circuits.

In this paper we extend this new reliability measure to sequential circuits. We present a new method for evaluation of signal reliability which can be applied to sequential as well as combinational circuits. The proposed algorithm evaluates the signal reliability in a recursive way and can easily be automated.

II. Basic Definitions and Assumptions

The reliability of a circuit depends upon the possible faults and their probabilities of occurrence. We assume that the possible faults are multiple faults of the stuck-at type, i.e., any line X in the circuit may be stuck at one (abbreviated s.a.1) or stuck at zero (s.a.0).

Let s_X denote the probability of occurrence of a single fault on line X. This fault can be either a s.a.0 fault with probability q_{0_X}, or a s.a.1 fault with probability q_{1_X}, satisfying:

$$s_X = q_{0_X} + q_{1_X}$$

The signal reliability of line X, designated R(X), is defined as follows:

R(X) = Pr{The logic signal on line X is correct}

Similarly, we define the signal unreliability, denoted Q(X):

Q(X) = Pr{The logic signal on line X is incorrect}

Clearly, $R(X) + Q(X) = 1$ (1)

Since the correct logic signal on line X can be either 0 or 1, we define the 0(1) signal reliability and the 0(1) signal unreliability as follows:[1]

$R_0(X)$ = Pr{Line X is correctly a 0}

$R_1(X)$ = Pr{Line X is correctly a 1}

$Q_0(X)$ = Pr{Line X is incorrectly a 0}

$Q_1(X)$ = Pr{Line X is incorrectly a 1}

Clearly, $R(X) = R_0(X) + R_1(X)$ (2)

and $Q(X) = Q_0(X) + Q_1(X)$ (3)

According to the method proposed in this paper, the signal reliabilities and unreliabilities of the lines in the circuit are evaluated recursively, i.e., the values of R_0, R_1, Q_0 and Q_1 for the output line of every subcircuit (a gate or a flip-flop) are calculated using the values of these reliability functions for its input lines. In order to simplify the equations relating the output and input signal reliabilities and unreliabilities of a subcircuit, we establish a simple model for the circuit. In this model we insert in each line of the circuit a special subnetwork called Fault Occurrence Network (abbreviated FON). Only in these special subnetworks may s.a.0 or s.a.1 faults occur, while the other parts of the circuit, i.e., the subcircuits and the primary input lines, are fault free. For example, the appropriate models for a NAND gate and a T flip-flop are shown in Fig. 1.

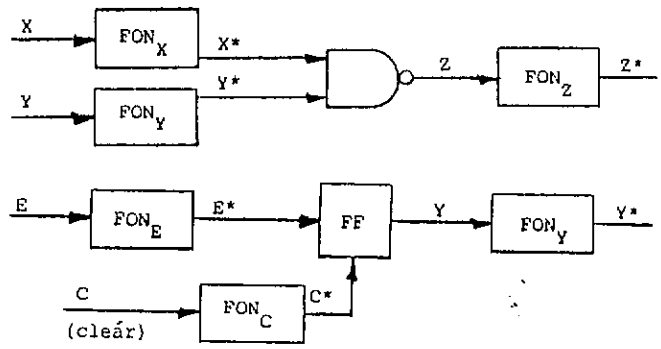

Fig. 1: The models for a NAND gate and a T-FF

The proposed model enables us to derive separately two sets of equations. The first set relates the output and input signal reliabilities and unreliabilities of a FON in a single line. The second set of equations relates the output and input signal reliabilities of a subcircuit which is fault free according to our model. The equations for gates are described in the next section, while the appropriate equations for flip-flops are described in Section IV.

We derive now the first set of equations for a single line. Let X* denote the output line of a FON

whose input line is X, and suppose that the values of $R_1(X)$, $R_0(X)$, $Q_1(X)$ and $Q_0(X)$ are given, thus:

$$R_1(X^*) = \Pr\{X^* \text{ is correctly a 1}\}$$

$$= \Pr\{X \text{ is correctly a 1} \cap \text{no fault occurred}\}$$

$$+ \Pr\{(X \text{ is correctly a 1 or incorrectly a 0}) \cap (\text{a s.a.1 fault occurred})\}$$

Since the occurrence of a fault in this line is independent of the correctness of the signal X, we obtain:

$$R_1(X^*) = R_1(X)\cdot(1-s_X) + [R_1(X) + Q_0(X)]q_{1_X}$$

Simple algebraic manipulations yield:

$$R_1(X^*) = R_1(X)\cdot(1-q_{0_X}) + Q_0(X)\cdot q_{1_X} \quad (4)$$

In a similar manner, we can prove the following equations:

$$R_0(X^*) = R_0(X)\cdot(1-q_{1_X}) + Q_1(X)\cdot q_{0_X} \quad (5)$$

$$Q_1(X^*) = Q_1(X)\cdot(1-q_{0_X}) + R_0(X)\cdot q_{1_X} \quad (6)$$

$$Q_0(X^*) = Q_0(X)\cdot(1-q_{1_X}) + R_1(X)\cdot q_{0_X} \quad (7)$$

If line X is a primary input line to the circuit, it is according to our assumptions fault free, hence:

$$Q_0(X) = Q_1(X) = 0$$

$$R_1(X) = \Pr\{X=1\} \qquad R_0(X) = \Pr\{X=0\} \quad (8)$$

The last two probabilities, denoted P_X and $1-P_X$, respectively, were called signal probabilities and were studied by Parker and McCluskey.[2,3] These signal probabilities can be caluclated for each line in the circuit, using the signal reliabilities and unreliabilities, as follows:

$$P_X = \Pr\{X=1\} = R_1(X) + Q_1(X) \quad (9)$$

$$1-P_X = \Pr\{X=0\} = R_0(X) + Q_0(X) \quad (10)$$

III. Signal Reliability of Combinational Circuits

Most combinational circuits are constructed out of basic gates like AND, OR, NAND, NOR and NOT. We will derive now, for all these kinds of basic gates, a single set of equations for calculating the output signal reliability. Each of these basic gates is a monotone gate whose logical operation can be described by a binary vector.[4] Let $X_1, X_2, \ldots, X_n$ denote the input lines of a monotone gate, and let Y denote the output line. This gate is described by the vector $(\alpha_1, \alpha_2, \ldots, \alpha_n, \beta)$, where $\alpha_1, \alpha_2, \ldots, \alpha_n$ is the only input combination for which the output equals β. For example, a three-input NOR gate is described by the vector (0001) since the gate output equals 1 only for the input combination (000) and equals 0 for any other input combination. The Boolean equation of a monotone gate can easily be derived from the corresponding vector in the following way:

$$Y^{\beta} = \bigcap_{i=1}^{n} X_i^{\alpha_i}$$

where $X^1 = X$ and $X^0 = \bar{X}$. For example, the Boolean equation derived from the vector (0001) is:

$$Y^1 = X_1^0 X_2^0 X_3^0 = \bar{X}_1 \bar{X}_2 \bar{X}_3 = \overline{(X_1+X_2+X_3)}$$

The equations for calculating the output signal reliabilities and unreliabilities of a monotone gate are given in the following theorem:

Theorem 3.1: The output signal reliabilities and unreliabilities of an n-input monotone gate, whose input signals $X_1, X_2, \ldots, X_n$ are independent, are given by the following equations:

$$R_{\beta}(Y) = \prod_{i=1}^{n} R_{\alpha_i}(X_i) \quad (11)$$

$$Q_{\beta}(Y) = \prod_{i=1}^{n} [Q_{\alpha_i}(X_i) + R_{\alpha_i}(X_i)] - R_{\beta}(Y) \quad (12)$$

$$Q_{\bar{\beta}}(Y) = \prod_{i=1}^{n} [Q_{\bar{\alpha}_i}(X_i) + R_{\alpha_i}(X_i)] - R_{\beta}(Y) \quad (13)$$

$$R_{\bar{\beta}}(Y) = 1 - [R_{\beta}(Y) + Q_{\beta}(Y) + Q_{\bar{\beta}}(Y)] \quad (14)$$

where $\alpha_1\alpha_2\ldots\alpha_n\beta$ is the binary vector describing this gate.

Proof: According to our model the gate is fault free, therefore:

$$R_{\beta}(Y) = \Pr\{Y \text{ is correctly a } \beta\}$$

$$= \Pr\{\text{Each } X_i \text{ is correctly an } \alpha_i\}$$

The n input signals are independent, hence:

$$= \prod_{i=1}^{n} \Pr\{X_i \text{ is correctly an } \alpha_i\} = \prod_{i=1}^{n} R_{\alpha_i}(X_i)$$

To prove equation (12) note that:

$$R_{\beta}(Y) + Q_{\beta}(Y) = \Pr\{Y \text{ is correctly or incorrectly a } \beta\}$$

$$= \Pr\{\text{Each } X_i \text{ is correctly or incorrectly an } \alpha_i\}$$

The independence between the input signals results in:

$$= \prod_{i=1}^{n} [R_{\alpha_i}(X_i) + Q_{\alpha_i}(X_i)]$$

and equation (12) follows.

In a similar manner we prove equation (13):

$$R_{\beta}(Y) + Q_{\bar{\beta}}(Y) = \Pr\{Y \text{ is correctly a } \beta \text{ or incorrectly a } \bar{\beta}\}$$

$$= \Pr\{Y \text{ is correctly a } \beta \text{ or should be a } \beta\}$$

$$= \Pr\{\text{Each } X_i \text{ is correctly an } \alpha_i \text{ or should be an } \alpha_i\}$$

$$= \prod_{i=1}^{n} [R_{\alpha_i}(X_i) + Q_{\bar{\alpha}_i}(X_i)]$$

Since $R_{\beta}(Y) + R_{\bar{\beta}}(Y) + Q_{\beta}(Y) + Q_{\bar{\beta}}(Y) = 1$, equation (14) follows.
Q.E.D.

Example: We employ now equations (11)-(14) for calculating the output signal reliability of the NAND gate shown in Fig. 1, assuming that the primary input lines X and Y are independent. In order to compare the final results to those obtained in [1], we assume that all possible faults are equally likely, i.e.:

$q_0 = q_1 = \frac{s}{2}$ for all three lines in the circuit.

Substituting the signal reliabilities of the primary input lines (8) into equations (4)-(7) results in the following:

$$R_1(X^*) = p_X \cdot (1-\tfrac{s}{2}) \qquad Q_1(X^*) = (1-p_X) \cdot \tfrac{s}{2}$$

$$R_0(X^*) = (1-p_X)(1-\tfrac{s}{2}) \qquad Q_0(X^*) = p_X \cdot \tfrac{s}{2}$$

Similar results are obtained for Y^*. Substituting these values into equations (11)-(14) yields:

$$R_0(Z) = R_1(X^*)\, R_1(Y^*) = p_X\, p_Y\, (1-\tfrac{s}{2})^2$$

$$Q_0(Z) = Q_1(X^*)\, R_1(Y^*) + Q_1(X^*)\, Q_1(Y^*) + R_1(X^*)\, Q_1(Y^*)$$

$$= \tfrac{1}{4} s^2 + (p_X + p_Y)\, \tfrac{s}{2}\, (1-s) + p_X\, p_Y\, (\tfrac{3}{4} s^2 - s)$$

$$Q_1(Z) = Q_0(X^*)\, R_1(Y^*) + Q_0(X^*)\, Q_0(Y^*) + R_1(X^*)\, Q_0(Y^*)$$

$$= p_X\, p_Y\, (s - \tfrac{1}{4} s^2)$$

$$R_1(Z) = R_0(X^*) + R_0(Y^*) - R_0(X^*)\, R_0(Y^*)$$

$$+ Q_0(X^*)\, Q_1(Y^*) + Q_1(X^*)\, Q_0(Y^*)$$

$$= (1 - \tfrac{1}{4} s^2) + (p_X + p_Y)\, \tfrac{s}{2}\, (s-1)$$

$$+ p_X\, p_Y\, (s - 1 - \tfrac{3}{4} s^2)$$

Equations (4)-(7) may be employed now to calculate $R_1(Z^*)$, $R_0(Z^*)$, $Q_1(Z^*)$ and $Q_0(Z^*)$. However, a simpler equation can be used in this example where only the value of $R(Z^*) = R_0(Z^*) + R_1(Z^*)$ has to be calculated. This simpler equation is derived by adding equations (4) and (5), and substituting $q_0 = q_1 = s/2$:

$$R(Z^*) = \tfrac{s}{2} + (1-s)\, R(Z)$$

Using this equation we obtain

$$R(Z^*) = (1 - \tfrac{s}{2} - \tfrac{s^2}{4} + \tfrac{s^3}{4}) + (p_X + p_Y)(s^2 - \tfrac{s}{2} - \tfrac{s^3}{2})$$

$$+ p_X\, p_Y\, (\tfrac{s^3}{2} - \tfrac{s^2}{2}) \qquad (15)$$

If all input combinations are equally likely, then $p_X = p_Y = 1/2$, and

$$R(Z^*/p_X = p_Y = 1/2) = 1 - s + \tfrac{5}{8} s^2 - \tfrac{1}{8} s^3$$

This is identical to the result obtained by Ogus.[1]

Using equation (15) for $R(Z^*)$, the output signal reliability can be calculated for any input combination by substituting $p_X = 1(0)$ for any input line satisfying $X = 1(0)$. For example, if XY = 00, then $R(Z^*/p_X = p_Y = 0) = 1 - s/2 - s^2/4 + s^3/4$. It can easily be verified that $R(Z^*/p_X = p_Y = 1/2)$ is the average of the four different values for $R(Z^*)$, corresponding to the four different input combinations.

Equations (11)-(14) can be employed for signal reliability calculations in any fan-out-free circuit where the input signals to each gate are independent. The main problem in extending these equations to general combinational circuits is the existence of reconverging fan-out lines causing dependencies between gate input signals. A similar problem concerning signal probabilities was studied by Parker and McCluskey.[3] They presented the following equations for the case where the signals are independent:

$$Pr\{\bar{A}=1\} = 1 - Pr\{A=1\} \qquad (16)$$

$$Pr\{AB=1\} = Pr\{A=1\} \cdot Pr\{B=1\} \qquad (17)$$

$$Pr\{A+B=1\} = Pr\{A=1\} + Pr\{B=1\} - Pr\{A=1\} \cdot Pr\{B=1\} \qquad (18)$$

It was suggested in [3] that these equations can be used in the case where the signals are dependent by suppressing the resulting exponents of the signal probabilities. This is illustrated in the following example:

Example: The circuit shown in Fig. 2 has three primary input lines, of which X_2 is a reconverging fan-out line causing dependency between the signals V and W. We will compute the output signal probability of this circuit in two different ways: First, by taking into account the dependency between the input signals V and W to the last AND gate, and second, by using equations (16)-(18) and suppresing exponents.

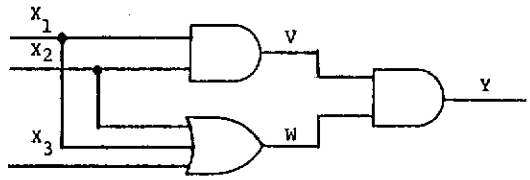

Fig. 2: An Example circuit.

The primary input lines are independent, therefore:

$$Pr\{V=1\} = Pr\{X_1=1\} \cdot Pr\{X_2=1\} = p_{X_1} \cdot p_{X_2}$$

$$Pr\{W=1\} = Pr\{X_2 + X_3 = 1\} = p_{X_2} + p_{X_3} - p_{X_2} \cdot p_{X_3}$$

Using the definition of signal probability, we obtain:

$$Pr\{Y=1\} = Pr\{VW=1\} = Pr\{X_1 X_2 (X_2+X_3)=1\}$$

$$= Pr\{X_1 X_2 = 1\} = p_{X_1} \cdot p_{X_2}$$

If we use equation (17) we obtain:

$$Pr\{Y=1\} = Pr\{VW=1\} = Pr\{V=1\} \cdot Pr\{W=1\}$$

Substitution yields:

$$= p_{X_1} p_{X_2} (p_{X_2} + p_{X_3} - p_{X_2} p_{X_3})$$

$$= p_{X_1} p_{X_2}^2 + p_{X_1} p_{X_2} p_{X_3} - p_{X_1} p_{X_2}^2 p_{X_3}$$

Suppressing the exponents of p_{X_2} (the signal probability of the reconverging fan-out line) results in:

$$Pr\{Y=1\} = p_{X_1} \cdot p_{X_2}$$

We shall now state formally the above.

Theorem 3.2: The output signal probability of a monotone gate whose input signals are dependent can be computed by using equations (16)-(18) and suppressing

the resulting exponents of the fan-out signal's probabilities.

Proof: Omitted for the sake of brevity.

In the following theorem we show that the principle of exponent suppression can be used in signal reliability calculations as well.

Theorem 3.3: The output signal reliabilities and unreliabilities of a monotone gate whose input signals are dependent can be calculated using equations (11)-(14) and suppressing the exponents of the fan-out signal's reliabilities and unreliabilities.

Proof: Using the method suggested by Ogus we can form for every circuit with output signal Z a new circuit with output signal H satisfying:[1]

$\Pr\{H=1\} = \Pr\{Z \text{ is correctly a } 1\} = R_1(Z)$

In a similar way we can form circuits satisfying

$\Pr\{H=1\} = R_0(Z)$ or $\Pr\{H=1\} = Q_1(Z)$ or $\Pr\{H=1\} = Q_0(Z)$.

According to Theorem 3.2, the probability $\Pr\{H=1\}$ can be calculated using the principle of exponent suppression. Consequently, this principle can be employed in signal reliability and unreliability calcualtions as well.
Q.E.D.

The following two examples illustrate the calculation of signal reliabilities of general combinational circuits.

Example: The Boolean function $f(X_1,X_2,X_3) = \Sigma(0,1,7)$ can be realized in two different ways, as shown in Fig.3. The first is a sum-of-products realization $N_1 = \bar{X}_1\bar{X}_2 + X_1X_2X_3$. The second is a product-of-sums realization $N_2 = (X_1 + \bar{X}_2)(\bar{X}_1 + X_2)(\bar{X}_1 + X_3)$. The output signal reliabilities of these two circuits were computed using an APL program. In these computations we assumed that all possible faults are equally likely, i.e., $q_0=q_1=s/2$ for all lines, and that $P\{X_1=1\} = P\{X_2=1\} = P\{X_3=1\} = 0.5$, i.e., all input combinations are equally likely. The results are plotted in Fig. 4 as a function of the fault probability s.

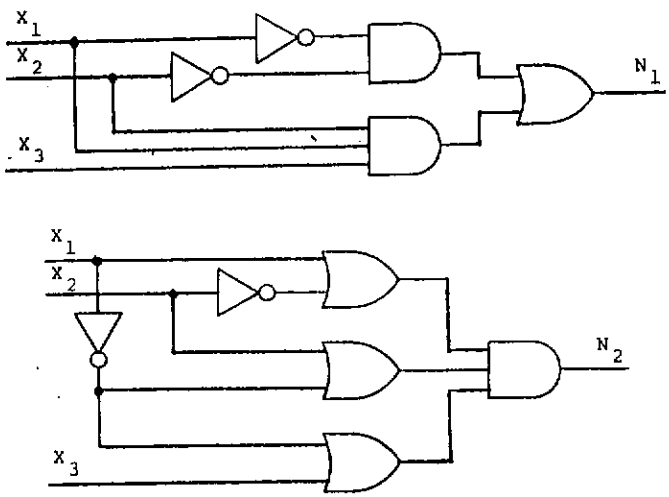

Fig. 3: Two realizations of the function

$$f(X_1,X_2,X_3) = \Sigma(0,1,7) .$$

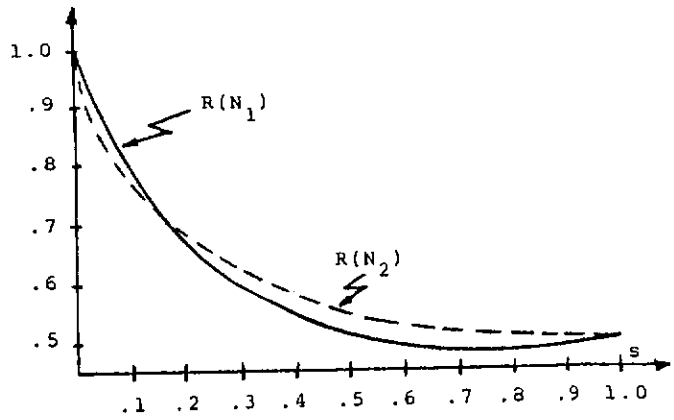

Fig. 4: The signal reliabilities of the circuits in Fig. 3.

Several conclusions can be drawn from this example. The main conclusion is that the output signal reliability of a circuit depends upon its structure. Hence, for a given Boolean function, we can compare several possible realizations and choose the one yielding the maximal output signal reliability. Another conclusion is that a circuit having a larger number of gates and lines and, consequently, a larger number of possible faults, is not necessarily less reliable, e.g., in the example the circuit N_2 has a larger number of gates and lines, however $R(N_2) > R(N_1)$ for $0.145 < s < 1.0$.

Another application of signal reliability calculations is to evaluate the increase or decrease in reliability caused by using TMR configurations, as shown in the following example.

Example: A binary Full-Adder is realized in a TMR configuration as shown in Fig. 5. We assume that multiple stuck-at-type faults may occur in the internal lines of the voter as well as in the internal lines of the FA modules.

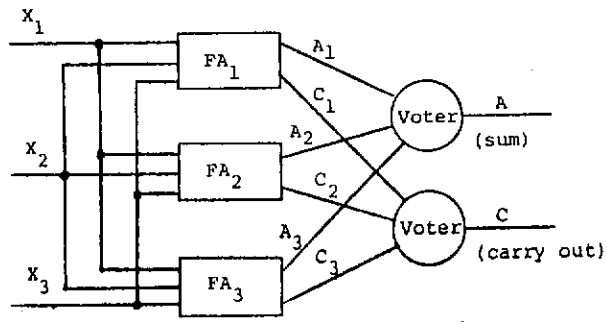

Fig. 5: A TMR configuration of a Full-Adder.

The signal reliabilities of the lines A_1, C_1, A and C were computed assuming that the probabilities of all possible faults are equal and that all input combinations are equally likely. The results are plotted in Fig. 6 as a function of the fault probability s.

The most interesting conclusion from this example is that if $s > 0.165$, the usage of a TMR configuration will decrease the signal reliability of both output lines instead of increasing them. However, for $s < 0.11$, the signal reliabilities of the sum and carry-out signals are increased by using a TMR configuration.

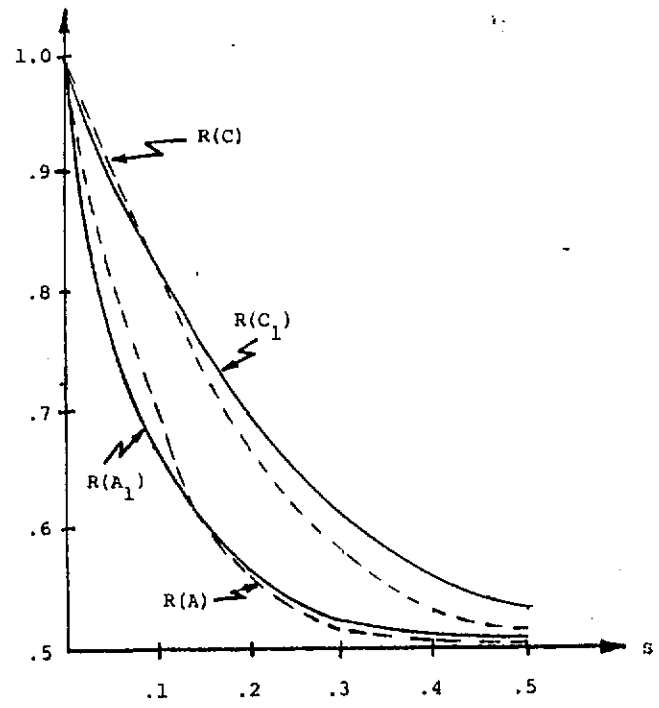

Fig. 6: The signal reliabilities of the TMR configuration in Fig. 5.

IV. Signal Reliability of Sequential Circuits

In this section we generalize the previous method for evaluating signal reliabilities to sequential circuits. To simplify notation, we assume that we are given a synchronous sequential circuit, shown in Fig. 7 with a single-input line X and a single-output line Z.

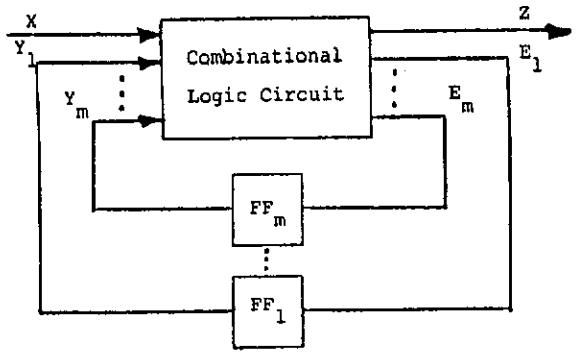

Fig. 7: A sequential circuit.

The circuit contains m flip-flops with excitation input lines $E_1, E_2, \ldots, E_m$ and output lines $Y_1, Y_2, \ldots, Y_m$, respectively.

Let $X^{(i)}$ and $Z^{(i)}$ denote the input and output signals of the circuit at time t_i, respectively. Let $E_1^{(i)}, \ldots, E_m^{(i)}$ and $Y_1^{(i)}, \ldots Y_m^{(i)}$ denote the input and output signals of the flip-flops at time t_i, respectively.

We wish to evaluate the signal reliabilities of $Z^{(i)}$ for $i = 1,2,\ldots,k$, where k is the length of the applied input sequence. Since $Z^{(i)}$ is an output signal of a combinational circuit, we can employ equations (11)-(14) for calculating the signal reliability of $Z^{(i)}$ (and $E_1^{(i)}, \ldots, E_m^{(i)}$ as well) if we are given the signal reliabilities of the current input $X^{(i)}$ and of $Y_1^{(i)}, Y_2^{(i)}, \ldots, Y_m^{(i)}$. The required signal reliabilities of $Y_1^{(i)}, \ldots, Y_m^{(i)}$ will be calculated in a recursive way, i.e., we will derive equations for calculating these signal reliabilities using the signal reliabilities of $Y_1^{(i-1)}, \ldots, Y_m^{(i-1)}$ and $E_1^{(i-1)}, \ldots, E_m^{(i-1)}$.

The exact form of the required equations depends upon the type of flip-flop used. In the following, we derive the appropriate equations for T flip-flops. The equations for other types of flip-flops may be derived in a similar way.

We derive now the equations for a single T flip-flop, and to simplify notation let $E^{(i-1)}$ and $Y^{(i-1)}$ denote the input and output signals at time t_{i-1}, respectively. The next state $Y^{(i)}$ of the T-FF is given by the following equation:

$$Y^{(i)} = Y^{(i-1)} \oplus E^{(i-1)}$$

where $\oplus$ represents the Exclusive OR operation; consequently, the following equations may also be employed for Exclusive OR gates. The 0-signal reliability of $Y^{(i)}$ is:

$$R_0(Y^{(i)}) = \Pr\{Y^{(i)} \text{ is correctly a 0}\}$$
$$= \Pr\{\text{Both } Y^{(i-1)} \text{ and } E^{(i-1)} \text{ are correctly a 0 or correctly 1 or incorrectly 0 or incorrectly 1}\}$$

Since these four events are disjoint, we obtain:

$$R_0(Y^{(i)}) = R_0(Y^{(i-1)})R_0(E^{(i-1)}) + R_1(Y^{(i-1)})R_1(E^{(i-1)}) + Q_0(Y^{(i-1)})Q_0(E^{(i-1)}) + Q_1(Y^{(i-1)})Q_1(E^{(i-1)}) \quad (20)$$

In a similar way we obtain:

$$R_1(Y^{(i)}) = R_0(Y^{(i-1)})R_1(E^{(i-1)}) + R_1(Y^{(i-1)})R_0(E^{(i-1)}) + Q_0(Y^{(i-1)})Q_1(E^{(i-1)}) + Q_1(Y^{(i-1)})Q_0(E^{(i-1)}) \quad (21)$$

$$Q_0(Y^{(i)}) = R_0(Y^{(i-1)})Q_0(E^{(i-1)}) + Q_0(Y^{(i-1)})R_0(E^{(i-1)}) + R_1(Y^{(i-1)})Q_1(E^{(i-1)}) + Q_1(Y^{(i-1)})R_1(E^{(i-1)}) \quad (22)$$

$$Q_1(Y^{(i)}) = R_0(Y^{(i-1)})Q_1(E^{(i-1)}) + Q_1(Y^{(i-1)})R_0(E^{(i-1)}) + R_1(Y^{(i-1)})Q_0(E^{(i-1)}) + Q_0(Y^{(i-1)})R_1(E^{(i-1)}) \quad (23)$$

Equations (20)-(23) can be used for calculating the signal reliability and unreliability of $Y^{(i)}$ for $i=2,3,\ldots,k$ if the signal reliability and unreliability of the initial state $Y^{(1)}$ of the FF are given. If these values are not given, different assumptions can be made regarding them. In the following we present three different situations in which the signal reliabilities of $Y^{(1)}$ are not given, and we suggest appropriate values for each case.

In the first case, the initial state of the FF is unknown. An appropriate assumption for this case is the following:

$$R_0(Y^{(1)}) = R_1(Y^{(1)}) = 1/2$$
$$Q_0(Y^{(1)}) = Q_1(Y^{(1)}) = 0 \qquad (24)$$

In the second case, the initial state is known, but no information regarding the signal reliabilities is available. If the initial state of the FF is α (α=0,1), $Y^{(1)}$ can be correctly an α or incorrectly an $\bar{\alpha}$, hence we assume:

$$R_\alpha(Y^{(1)}) = Q_{\bar{\alpha}}(Y^{(1)}) = 1/2$$
$$R_{\bar{\alpha}}(Y^{(1)}) = Q_\alpha(Y^{(1)}) = 0$$

In the third case, a clear signal is applied to the FF, thus the initial state is known and its signal reliability can be calculated. The results obtained for a T-FF with clear input C are:

$$R_0(Y^{(1)}) = 1 - \frac{1}{2} q_{0_C} \qquad Q_1(Y^{(1)}) = \frac{1}{2} q_{0_C}$$
$$R_1(Y^{(1)}) = Q_0(Y^{(1)}) = 0$$

Example: A serial binary adder is shown in Fig. 8. This sequential circuit has two primary input lines and contains a single T-FF with a clear input. The signal reliability of $Z^{(1)} = Z(t_1)$ and $Z^{(2)} = Z(t_2)$ were computed for all possible input sequences assuming that a clear signal preceded every input sequence and that all possible faults are equally likely, i.e., $q_0 = q_1 = 0.05$ for all the lines in the circuit. Some of the results are summarized in Table I. From these results we can see that the output signal reliability function is not necessarily a decreasing function and that there are input sequences for which $R(Z^{(2)}) > R(Z^{(1)})$.

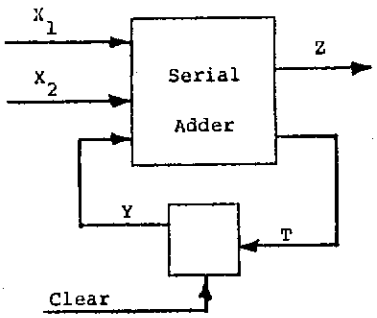

Fig. 8: A Serial Adder.

TABLE 1: Output signal reliability of a serial adder

	t_1	t_2	t_1	t_2
Input sequence	00	00	00	01
Output signal reliability	0.6571	0.5359	0.6571	0.6979
Input sequence	01	11	11	11
Output signal reliability	0.7749	0.4784	0.6250	0.8399

V. Conclusions

A recursive procedure for calculating the output signal reliability of combinational and sequential circuits has been developed in this paper. This procedure requires the performing of very simple operations which are easily automated.

As mentioned in [1] and [3], there are many applications of the signal reliability measure. The procedure presented in this paper simplifies the computations involved and extends the usage of this measure to sequential circuits. Moreover, the basic equations presented in this paper can be used to establish appropriate equations relating the output and input signal reliabilities of standard modules (combinational or sequential), rather than simple subcircuits (gates or flip-flops). Thus, the amount of computation involved in evaluating signal reliabilities of large circuits, which are constructed out of these standard modules, will be considerably reduced.

These extensions and other possible applications of the signal reliability measure will be presented in a subsequent paper.

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Israel Koren is an Assistant Professor in the Electrical Engineering and Computer Science Department at the University of California, Santa Barbara. He received the B.Sc. (Cum laude), M.Sc. and D.Sc. degrees from the Technion - Israel Institute of Technology, Haifa, in 1967, 1970 and 1975, respectively, all in Electrical Engineering.

From 1968 to 1971, he was with the Computer Center, Israel Ministry of Defense. In 1972, he joined the Electrical Engineering Department at the Technion, where he became a lecturer in 1975. He was also a consultant to the computer industry involved in R&D projects, mainly computer interfacing and data communication terminals. His research interests include Switching Theory, Finite Automata, Fault-Tolerant Computing, Computer Architecture and related subjects. Dr. Koren is a member of IEEE.