# Yield Enhancement vs. Performance Improvement in VLSI Circuits*

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*ABSTRACT*

For advanced submicron VLSI technologies maintaining higher performance and better yield is a challenging task. Layout optimization for improving yield may affect the circuit performance and vice versa. We analyze the effect of layout modifications for parasitic capacitance reduction on yield in this paper. Our results show that the solutions to the yield enhancement and parasitic capacitance reduction problems are very close to each other.

## I. Introduction

After minimizing the layout area during VLSI layout synthesis, it is still possible to further optimize the layout for improved performance, yield, and other manufacturability objectives. Several yield enhancement techniques have been developed for the last two stages of VLSI design, i.e., topological/symbolic layout design and physical layout design [2, 3, 4]. The approach is based on modifications of the layout to reduce the sensitivity of the chip to point random defects without increasing the area.

Wire-length minimization (WLM) is a commonly-used secondary optimization performed in the compaction stage of the layout synthesis for better electrical performance due to improvements in $RC$ characteristics. Several algorithms have been proposed for WLM [6, 7] and they have been implemented in commercial CAD systems. However, for VLSI technologies with feature sizes smaller than 0.5 microns, simple wire length minimization may not guarantee performance improvements. In submicron technologies interconnect delay can be dominated by cross-coupling capacitance between adjacent signal lines. Recently, spacing algorithms have been proposed for minimizing the interconnect delay [8].

Often layout modifications for optimizing one parameter might affect the other parameters. For example, when the width of the interconnect wire is increased in order to decrease the sensitivity to open-circuit type defects, the resistive load will increase which is undesirable. However, when the spacing between two long adjacent interconnect wires is increased, for reducing the sensitivity to short-circuit type defects, it will also decrease the cross-coupling capacitance between them. Therefore, layout modifications for yield enhancement might influence the parasitic capacitive loads. In this paper, we analyze the impact of layout modifications for reducing cross-coupling capacitance on yield.

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## II. Performance and Yield

The layout compaction algorithm presented in [2] improves the yield of the final design by distributing the spacing among non-critical (spatial) layout patterns so as to minimize the total sensitivity to short-circuit type defects for given particular manufacturing conditions, i.e., defect size distribution and defect densities. The sensitivity to open-circuit type defects is minimized by increasing the width of several non-critical patterns in the layout. Some routing techniques for yield enhancement have been developed for two-layer routing [4, 9]. These routing algorithms are also based on the minimization of the sensitivity of the layout to defects.

In highly integrated systems interconnect delay can be a limiting factor for achieving high performance. Therefore, during circuit and layout design, interconnect wire length is minimized in order to achieve better performance and lower power. The trade-off between wire length minimization and yield enhancement is analyzed in [3]. In wire length reduction only the area/length of the layout patterns is considered whereas for yield enhancement both the area of the layout patterns and the spacing among them must be considered. In [3], it has been shown that layout modifications for yield enhancement also reduce wire length, which benefits performance.

During wire length minimization, the effect of cross-coupling capacitance is often ignored. However, in submicron technologies interconnect delay can be dominated by cross-coupling capacitance between adjacent signal lines. In [8] it has been shown that delay can be reduced by 5% when the layouts of 0.5 micron technology are optimized based on coupling capacitance. The crosstalk also

has been reduced by about 15-20% due to reduction in the coupling capacitance. They found that by increasing the layout area, further improvements in delay can be achieved.

### A. Interconnection Capacitance

The interconnect wire capacitance consists of area (parallel plate) capacitance and wire to wire coupling capacitance. The area capacitance depends on the length, width and thickness of the wire and insulator (oxide). The cross-coupling capacitance depends on the wire dimensions as well as the spacings between adjacent interconnect lines [1, 10]. The models for the ground and cross-coupling capacitance are given below.

$$C_{gnd} = \epsilon_{ox}\left\{1.15\left(\frac{W}{H}\right) + 2.80\left(\frac{T}{H}\right)^{0.222}\right\} \quad (1)$$

$$C_x = \epsilon_{ox}\left\{1.93\left(\frac{T}{H}\right)^{1.1} + 1.14\left(\frac{W}{H}\right)^{0.31}\right\}\left(\frac{S}{H} + 0.51\right)^{-1.45} \quad (2)$$

where $C_{gnd}$ is the capacitance to the ground plane, $C_x$ is the cross-coupling capacitance, $\epsilon_{ox}$ is the dielectric constant of the oxide, $T$ is the thickness of the interconnect wire, $H$ is the thickness of the oxide, $W$ is the width of the wire and $S$ is the spacing between the two conducting wires. These parameters are illustrated in Figure 1.

The plots of the interconnect wire capacitance are shown in Figure 1. The wire capacitance to ground ($C_{gnd}$) is larger than the cross-coupling capacitance ($C_x$) between conductors, when the wire width ($W$) is larger than the oxide thickness ($T$). $C_x$ dominates when $W$ is smaller than $T$. The cross-over point is at $W/T = 1.2$.

The minimum feature size of the interconnect wires has been scaled down to 0.3-0.5 microns in the current technologies. However, thickness of the wires and insulating oxide has not been scaled down to the same level. Therefore, the ratio of the thickness of wire and insulator has already reached the cross-over point where the cross-coupling capacitance is larger than the ground capacitance. Therefore, there is a need to consider the cross-coupling capacitance during the layout optimization. We illustrate the differences in the layout when it is optimized for yield, wire length and cross-coupling capacitance through a simple example in the next section.

### B. Yield vs. Cross-coupling Capacitance

In case of yield enhancement the optimal location for a layout element depends on its length and the spacing to the elements above and below. In addition, elements connected on both sides and their width also influence the optimal location of an element [2]. In Figure 2(a) segment $A1$ has 30 units of slack to begin with. The spacing between the segments $A1$ and $C$ is the minimum design rule

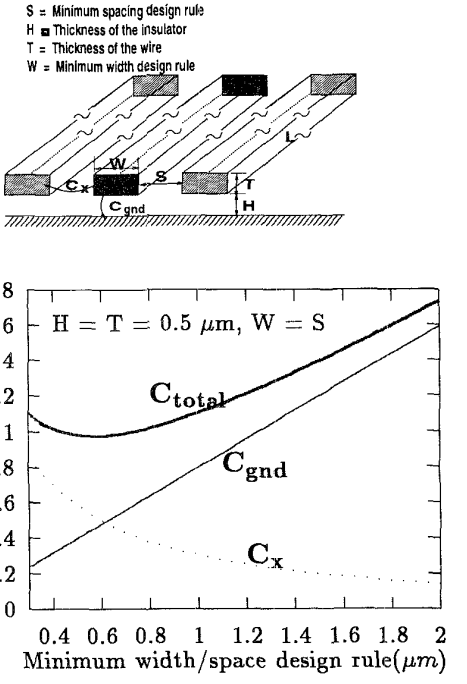


Figure 1: Interconnect wire capacitance.

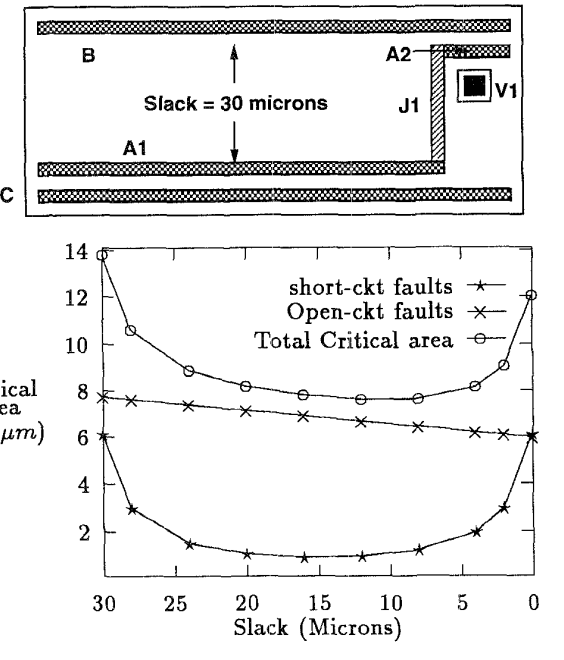


Figure 2: Layout optimization for yield enhancement. (a) Layout before relocating segment $A1$ (b) Critical area vs slack.

spacing whereas the spacing between the segments $A1$ and $B$ is 30 units more than the minimum required.

In the initial position the critical area of segment $A1$ and jog $J1$ is 13.8 sq. $\mu$m. The segment $A1$ is moved upwards by a step size, i.e., 1 unit at a time and the critical area is calculated. Critical area of both short- and open-circuit faults is reduced until $A1$ is moved to the center, i.e., 15 units upwards. The critical area for short-circuit faults is reduced because the available spacing is uniformly distributed. The critical area for open-circuit faults is reduced because now the jog length is halved. Beyond this, when $A1$ is further moved upwards, the critical area for short-circuit faults is higher. However, this increase is compensated by reduction in the critical area for open-circuit faults of jog $J1$. As shown in Figure 2(b), the critical area is reduced to a minimum after moving $A1$ 20 units upwards. Therefore, the optimal location for segment $A1$ is 10 units below segment $B$ as shown in Figure 3(a).

Now segment $A1$ is relocated from the initial position for reducing the total parasitic capacitance instead of yield optimization. As shown in equation 2, both layout pattern dimensions and spacings, as in the case of yield optimization, must be considered for minimizing the total interconnect capacitance [8]. If the layout shown in Figure 2(a) is optimized for parasitic capacitance (ground and cross-coupling) reduction, the optimal location for segment $A1$ is 8 units below segment $B$. As segment $A1$ is moved upwards both cross-coupling and parallel plate capacitance are reduced as shown in Figure 3(b). The total capacitance is minimum when segment $A1$ is 8 units below segment $B$. In case of WLM, since only the parallel plate capacitance (and resistance) is considered, its minimum is achieved when segment $A1$ is moved all the way up. It is to be noted that for these technologies the yield optimization solution may result in better performance when compared with that of the WLM solution. In case of WLM solution the total capacitance is 0.195 pf (Figure 3(b)) whereas in yield enhancement solution it is 0.14 pf which is very close to its minimum (0.138 pf).

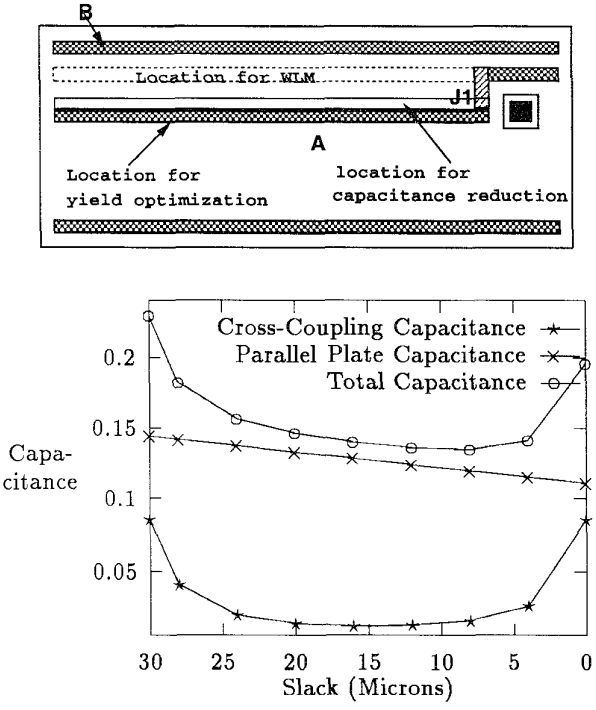


Figure 3: Layout optimization for parasitic capacitance (a) Optimized layout (b) Capacitance vs slack.

## III. Examples

The yield enhancement and parasitic capacitance reduction algorithms are implemented in a constraint-graph based compactor. A two-layer channel routing layout is optimized for yield and parasitic capacitance separately and the defect sensitivity of the optimized layouts are compared in this section.

The results of the layout optimization are shown in Figure 4. The uncompacted layout of Figure 4(a) is a part of the layout generated by the router of the MAGIC layout editor from the netlist of *example3b* of [11]. The layout shown in Figure 4(a) is generated by the compactor PLOW with automatic jog insertion, straightening and with minimum horizontal length of 12 $\Lambda$. The layouts optimized for yield and parasitic capacitance are shown in Figures 4(b) and 4(c), respectively.

To characterize the impact of the layout optimization on manufacturing yield, the yield analysis tool XLASER [5] was used. Probability of failure versus defect size plot is shown in Figure 5 for short-circuit faults of the metal-1 layer. The average probability of a short-circuit type failure in the metal-1 layer of the original compacted layout is 0.00119. This probability is reduced by 18.5% to 0.00097. On the other hand when the layout is optimized for parasitic capacitance reduction, the fault probability is reduced by 16.8% to 0.00099. The difference in the defect sensitivity of the layouts is very minimal. Both layouts are very similar, except for the spacing between some layout patterns.

Through the above example it has been demonstrated that in the submicron VLSI technologies, layout modifications for yield enhancement will not degrade the circuit performance. If the cross-coupling capacitance is also taken into account, layouts synthesized for improved performance are very close to that of yield solutions.

## IV. Conclusions

A channel routing benchmark layout is optimized for yield and cross-coupling capacitance and the defect sensitivity characteristics of the optimized layouts are compared. It has been demonstrated that for the submicron VLSI tech-

nologies, layout modifications for yield enhancement will also improve the circuit performance due to reduced coupling capacitance. In timing driven layout synthesis, it is possible to apply these two optimizations selectively to various parts of the design and thereby achieve optimal results.

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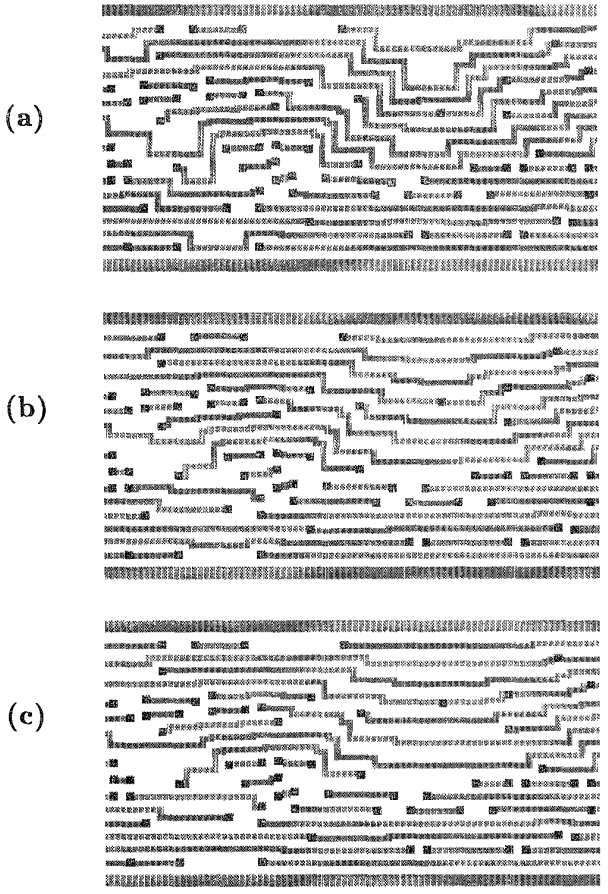


Figure 4: (a) Original Layout. (b) Layout optimized for yield. (c) Layout optimized for parasitic capacitance.

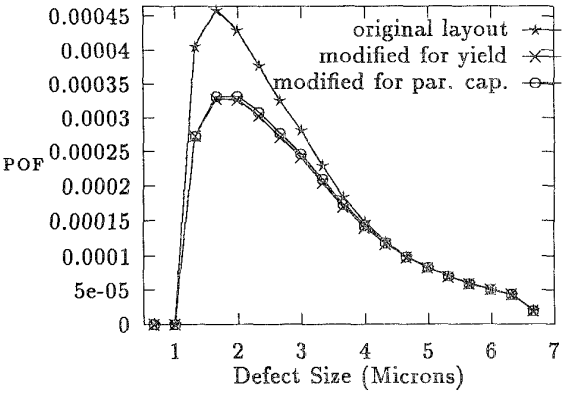


Figure 5: Probability of failure vs. Defect size of layout shown in Figure 4.