ECE 666 – Sample Exam

UNIVERSITY OF MASSACHUSETTS
Department of Electrical and Computer Engineering

<u>Computer Arithmetic - Mid-term II</u>

Open notes - 120 minutes. Solve all three problems. Write your answers in the provided space.

1. To speed-up the SRT algorithm for fast division (for a divisor in the range $[0.5,1]$) it has been suggested to use the first two bits of the divisor as a comparison constant K. For example, for $D = 0.1101$ the most significant bits of the partial remainder will be compared to $K = 0.11$.

(a) Will the number of add/subtract operations in the suggested method be smaller than, equal to, or greater than the number of these operations in the original SRT method (with $K = 0.1$) in the following three cases: (i) $D = 0.1001$ and $X = 0.10000111$; (ii) $D = 0.1101$ and $X = 0.01011011$; (iii) $D = 0.1111$ and $X = 0.01001011$

(b) Would you recommend the use of the above algorithm?

2. For single-precision floating-point operands in the IEEE format a 24×24 significand multiplier has to be designed using 8×8 multiplier library cells (with 16-bit result), (5,5,4) counters and a carry look-ahead adder.

(a) If all 48 bits have to be generated, how many 8×8 multipliers and (5,5,4) counters are needed?

(b) Assuming that the cell library includes 4-bit adders and a 4-bit carry-look-ahead module, how many such cells are needed to design the fastest carry look-ahead adder?

(c) If the product has to be represented in the single-precision IEEE floating-point format after rounding (to nearest-even), can some of the 8×8 multipliers and (5,5,4) counters be deleted? If your answer is negative explain why. If it is positive repeat part (a).

3. Prove that the arrangement of partial product bits shown below produces the correct product of two 5-bit two's complement operands, where $\overline{x}_i = 1 - x_i$ and similarly $\overline{a}_i = 1 - a_i$. Briefly ompare this multiplier to alternative two's complement array multipliers considering the amount of hardware and execution time.

					a_4	a_3	a_2	a_1	a_0
				$\times$	x_4	x_3	x_2	x_1	x_0
					$a_4 \cdot \overline{x}_0$	$a_3 \cdot x_0$	$a_2 \cdot x_0$	$a_1 \cdot x_0$	$a_0 \cdot x_0$
				$a_4 \cdot \overline{x}_1$	$a_3 \cdot x_1$	$a_2 \cdot x_1$	$a_1 \cdot x_1$	$a_0 \cdot x_1$	
			$a_4 \cdot \overline{x}_2$	$a_3 \cdot x_2$	$a_2 \cdot x_2$	$a_1 \cdot x_2$	$a_0 \cdot x_2$		
		$a_4 \cdot \overline{x}_3$	$a_3 \cdot x_3$	$a_2 \cdot x_3$	$a_1 \cdot x_3$	$a_0 \cdot x_3$			
	$a_4 \cdot x_4$	$\overline{a}_3 \cdot x_4$	$\overline{a}_2 \cdot x_4$	$\overline{a}_1 \cdot x_4$	$\overline{a}_0 \cdot x_4$				
	$\overline{a}_4$	0	0	0	a_4				
1	$\overline{x}_4$	0	0	0	x_4				
P_9	P_8	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0