FAULT TOLERANT SYSTEMS

http://www.ecs.umass.edu/ece/koren/FaultTolerantSystems

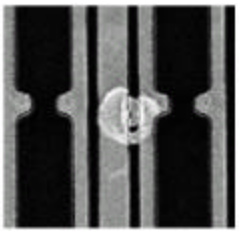
Part 19 – VLSI 1
Chapter 8 –Defect Tolerance in VLSI Circuits

Motivation for VLSI Defect Tolerance

- With increasing number and density of devices in VLSI chips - some imperfections inevitable
- These reduce the yield - proportion of operational circuits out of total number of fabricated circuits
- Defect tolerance techniques needed for yield enhancement
  - Making ICs less sensitive to manufacturing defects
  - Example techniques: Hardware redundancy, Layout modifications
- Redundancy increases chip area
  - More defects
  - Fewer chips per wafer
- Yield projections required to determine the optimal amount of redundancy

Manufacturing Defects

- Yield losses - caused mainly by
  - systematic defects (gross area defects)
  - random spot defects
- Systematic defects, e.g.,
  - parametric defects
  - mask misalignments
    - » dealt with during the fabrication process



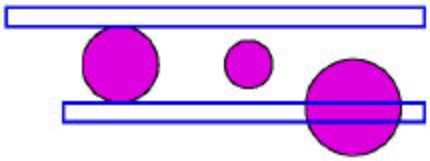
- Random spot defects
  - local contamination - mostly from undesired chemical and airborne particles deposited during various steps of process
  - cannot be totally eliminated
  - effect can be minimized during design process
- We focus mainly on spot defects
  - statistical modeling
  - ways to minimize their effect

Spot Defect Types

- Spot defects classification
  - Missing material - may result in open circuits
  - Extra patterns - may result in short circuits
  - Intra-layer defects - missing or extra material between adjacent wires
  - Inter-layer defects - missing or extra material between two separate layers
- Not all spot defects result in structural faults
- Only defects that turn into faults cause yield losses
- What is the percentage of defects that become faults ? (POF – probability of failure)

Defects Vs. Faults

- **Defect** - any imperfection on wafer
- **Fault** - a defect affecting circuit operation
- A **defect** causes a structural **fault** if it is large enough to connect two disjoint conductors or disconnect a continuous pattern
- Depends on location and size of defect, and on layout and density of circuit



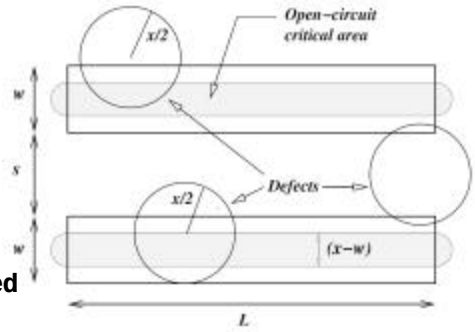
- **Example**: 3 extra material defects among metal conductors
  - two right ones will not short circuit any conductor
  - leftmost one causes a short circuit fault
- Only **faults** cause yield losses

Parametric faults

- Some defects do not cause structural (functional) faults - may still result in **parametric faults**
- Electrical parameters of some devices are outside desired operational window
- This affects the circuit performance
- **Example**: a missing-material defect too small to disconnect a transistor - may affect its performance
- May also be the result of global defects which cause variations in process parameters
- **We concentrate here on functional faults**

Probability of Failure (pof)

- **pof** - Fraction of defects which result in faults
- Depends on
  - defect type
  - defect size
  - circuit geometry
- **Simplifying assumption** - defect is circle shaped with diameter **x**
- Other shapes can be considered



- $q_i(x)$ - **pof** for a defect of type **i**, diameter **x**
- q_i - **pof** for type **i** defects
- q_i obtained by averaging $q_i(x)$ over **x**

Calculating pof

$$\theta_i = \int_{x_0}^{x_M} \theta_i(x)\, f_d(x)\, dx$$

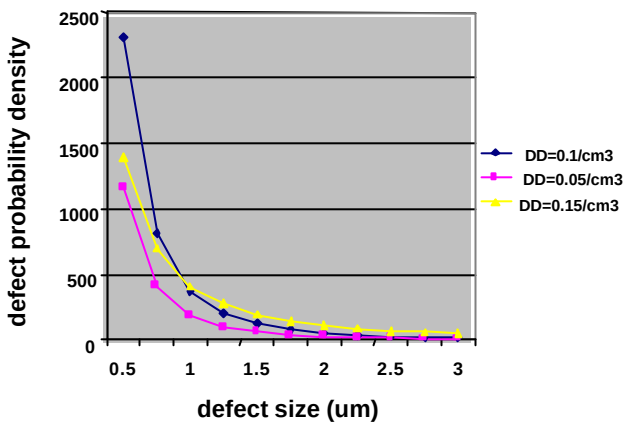
- $f_d(x)$ - probability density function of diameter **x**
- Based on experimental data:

$$f_d(x) = \begin{cases} \frac{k}{x^p} & \text{if } x_o \le x \le x_M \\ 0 & \text{otherwise} \end{cases}$$

and $$k = (p-1)x_0^{p-1}x_M^{p-1}/(x_M^{p-1} - x_0^{p-1})$$

- X_0, X_M - minimum, maximum size of defect
- **p** and X_M - determined empirically
- X_0 - resolution limit of lithography process
- Typically, $2 \le p \le 3.5$

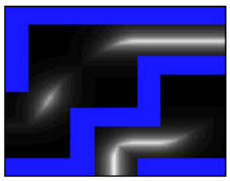
Defect Size Distribution



Critical Area and pof

- $A_i^{(c)}(x)$ - **critical area for defects of type i and diameter x - size of area in which center of a type i, diameter x defect must fall in order to cause circuit failure**
- $A_i^{(c)}$ - **average over all defect diameters x**

$$A_i^{(c)} = \int_{x_0}^{x_M} A_i^{(c)}(x)\, f_d(x)\, dx$$

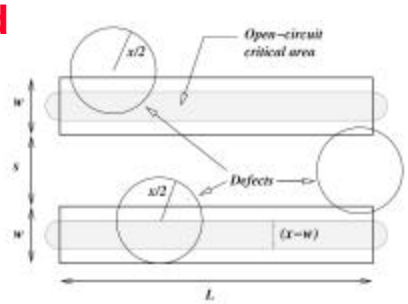


- **A_{chip} - chip area**

$$\theta_i(x) = \frac{A_i^{(c)}(x)}{A_{chip}} \qquad \theta_i = \frac{A_i^{(c)}}{A_{chip}}$$

- **Calculating critical area/pof**
  - **Geometry-based methods – calculate $A_i^{(c)}(x)$ first**
  - **Monte-Carlo methods - calculate $q_i(x)$ first**

Geometry-Based Method



- **Example : Critical area for size x missing-material defect in conductor of length L, width w = size of shaded area**

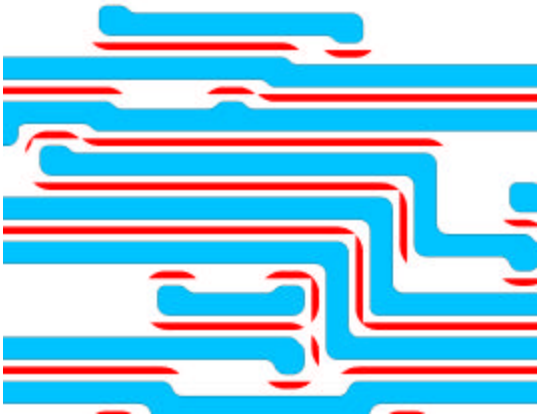
$$A_{miss}^{(c)}(x) = \begin{cases} 0 & \text{if } x < w \\ (x-w)L + \frac{1}{2}(x-w)\sqrt{x^2-w^2} & \text{if } x \geq w \end{cases}$$

- **Quadratic function of x – quadratic term negligible for L >> w**
- **Long conductors - linear term only**
- **$A_{extra}^{(c)}(x)$ for extra-material defects in a rectangular area of width s between two adjacent conductors - replace w by s**

Geometry-Based Methods - Cont.

- **Other regular shapes - analyzed similarly**
- **Common VLSI layouts - many shapes in different sizes/orientations**
- **Critical area difficult to derive**
- **Polygon expansion technique**
  - **Polygons expanded by x/2**
  - **Intersection of expanded polygons = critical area for short-circuit faults of diameter x**

Geometry-Based Methods - Illustration

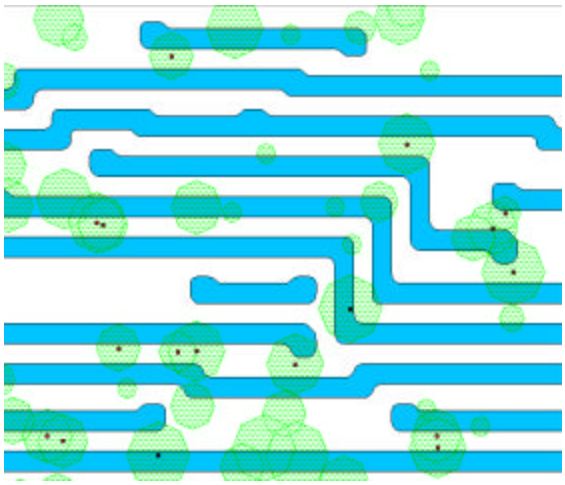


Critical Area for short circuit defects (in red)

Monte-Carlo-Based Method

- Simulated circles representing defects of different sizes are placed at random locations of layout
- For each "defect" - circuit of defective IC extracted and compared with defect-free circuit
- Determines whether defect results in a circuit fault
- Pof = $q_i(x)$ = fraction of type i, diameter x defects which would have resulted in a fault
- Averaged with respect to $f_d(x)$ - probability density function of diameter x - to produce q_i
- And, $A_i^{(c)} = \theta_i A_{chip}$
- Circuit fault resulting from a given defect is exactly identified
- Very time consuming - recently more efficient implementations have been developed

Monte-Carlo Critical Area Extraction



Octagonal defects

Short circuit defects are marked

Calculating Defect and Fault Densities

- d_i = average number per unit area (density) of defects of type i
- Average number of type i defects on chip = $A_{chip} \times d_i$
- Average number of type i faults on chip =

$$\theta_i A_{chip} d_i = A_i^{(c)} d_i$$

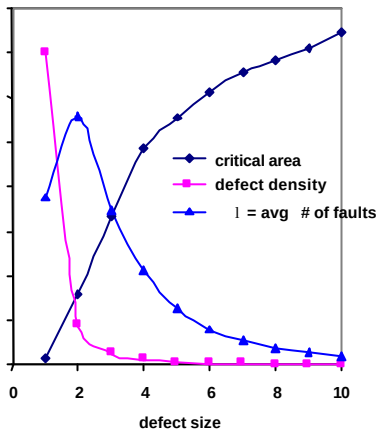
- λ = average number of all types of faults on chip = sum over all defect types i

$$\lambda = \sum_i A_i^{(c)} d_i = \sum_i \theta_i A_{chip} d_i$$

- λ is the parameter used in statistical yield modeling

Critical area, defect density, and fault density

- Critical area increases with defect size
- Defect density decreases sharply with defect size
- Therefore, peak fault density is usually for defect sized just over the minimum size



Yield Modeling

- l - the average number of **faults** - main parameter in yield modeling
- **Yield model** –
  - probabilistic model describing the distribution of **faults** over the chip
  - Uses the parameter l and possibly additional parameters
- **Simplistic models** – use l of the whole chip
- **Advanced models** – use l of chip component/layer

- **Which probabilistic model should be used?**

Basic Yield Models - Poisson Model

- X - number of faults on chip
- The Poisson Yield Model is the simplest yield model

$$\text{Prob}\,(X = k) = \frac{e^{-\lambda}\lambda^k}{k!}$$

- λ = average number of faults on chip
  = expected value of X
- If no defect/fault-tolerance exists -
  yield=Y_{chip}=prob. of no faults on chip=Prob(X=0)

$$Y_{chip} = \text{Prob}\,(X = 0) = e^{-\lambda}$$

Motivation for the Poisson Model

- Suppose chip area is divided into n small statistically independent sub-areas, each with probability λ/n of having a fault in it

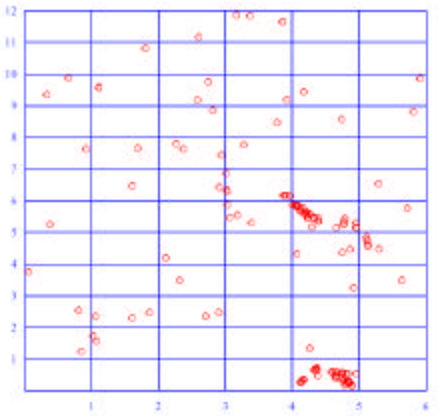
$$\text{Prob}\,(X = k) = \binom{n}{k}(\lambda/n)^k(1-\lambda/n)^{n-k}$$

- As the sub-areas become very small and $n \to \infty$

$$\text{Prob}\,(X = k) = \binom{n}{k}(\lambda/n)^k(1-\lambda/n)^{n-k} \to \frac{e^{-\lambda}\lambda^k}{k!}$$

This results in the Poisson Model

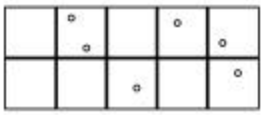
Actual Wafer Defect Map



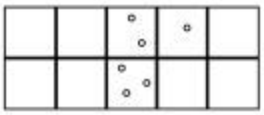
- Poisson model → sub-areas statistically independent → very low clustering
- Poisson model does not fit empirical data which tend to cluster

Effect of Fault Clustering on Yield

- Example:



(a) Non-clustered faults, $Y_{chip} = 0.5$



(b) Clustered faults, $Y_{chip} = 0.7$

- Increased clustering → higher yield
- Actual defects tend to cluster
- Poisson model pessimistic - predicted chip yields lower than actual manufacturing yields
- Modifications are proposed to Poisson model to account for fault clustering

Compound Poisson Models

- **Most common modification – compounding**
  - consider the fault density a random variable, not a constant
  - l is now the expected value of a random variable L with values l and density function $f_L(l)$ (compounder)
- **Averaging (compounding) with respect to $f_L(l)$ -**

$$\text{Prob}\,(X = k) = \int_0^\infty \frac{e^{-l}\, l^k}{k!} f_L(l)\, dl$$

- **Chip yield (no redundancy):** $Y_{chip} = \text{Prob}\,(X = 0) = \int_0^\infty e^{-l} f_L(l)\, dl$
- **Compounder $f_L(l)$ must satisfy**

$$\int_0^\infty f_L(l)dl = 1 \;\; ; \;\; E(L) = \int_0^\infty l f_L(l)dl = \lambda$$

- **Result - Compound Poisson distribution**
  - different sub-areas on chip are correlated
  - more pronounced clustering than generated by the Poisson distribution

Most Common Compounder

- **Most common compounding function - the Gamma distribution function with two parameters l and a**

$$f_L(l) = \frac{\alpha^\alpha}{\lambda^\alpha \Gamma(\alpha)} l^{\alpha-1} e^{-\frac{\alpha}{\lambda} l}$$

$$Prob(k\ Faults\ on\ Chip) = \frac{\Gamma(\alpha+k)}{k!\ \Gamma(\alpha)} \frac{(\lambda/\alpha)^k}{(1+\lambda/\alpha)^{\alpha+k}}$$

$$Chip\_Yield = Prob(0\ Faults\ on\ Chip) = (1+\lambda/\alpha)^{-\alpha}$$

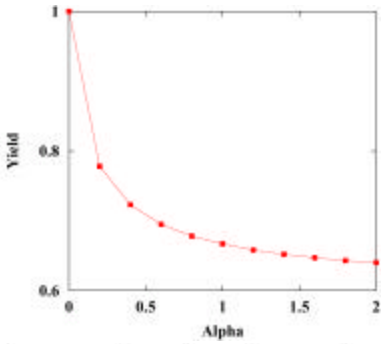
- **This is the Large-area Negative Binomial model**

Negative Binomial Distribution

- The whole chip constitutes one unit
- Subareas in chip are correlated with regard to faults
- Two parameters - more flexible and easier to fit to actual data than Poisson with one parameter
- λ - average number of faults per chip
- α - measure of amount of fault clustering
  - Smaller values of α indicate increased clustering
  - typical values for α - between **0.3** and **5**
  - As $\alpha \rightarrow \infty$, yield → Poisson yield – no clustering
- **The use of the Negative Binomial distribution for yield projection is now in practice, the industry standard**

Effect of Clustering Parameter α on Yield

- **Example 1:**
  Effect of α on chip yield for λ=**0.5**



- **Example 2:**
  Projecting yield of future products; λ selected so that the initial yield is **0.6**

α	A_0	$8A_0$
0.25	0.6	0.368
1	0.6	0.158
2	0.6	0.090
∞	0.6	0.017

1st Variation – include Gross Yield Factor

- Including the effect on yield of systematic defects in addition to spot defects
- Y_0 - gross yield factor - probability of no systematic defects on chip

$$Chip\_Yield = Y_0\left(1+\frac{l}{a}\right)^{-a}$$

Negative Binomial Distribution – 2nd Variation

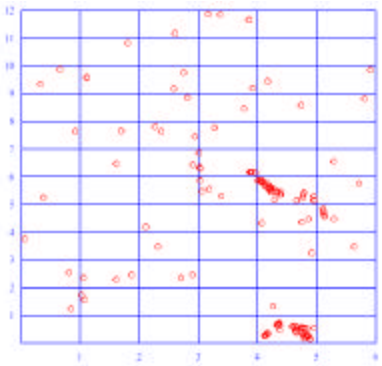
- Varying fault densities for different chip components/layers/fault type
- l_i - average number of faults for i-th component/layer/fault type with a clustering parameter a_i

$$Chip\_Yield = \prod_i \left(1+\frac{l_i}{a_i}\right)^{-a_i}$$

Negative Binomial Distribution – 3rd Variation

- Fault clusters smaller than chip
  - Medium Size Clustering
    - Chip is divided into B blocks » size of cluster
    - l/B - average number of faults in block

$$Chip\_Yield = \prod_{i=1}^{B}\left(1+\frac{l_i}{a_i}\right)^{-a_i}$$



Parameter Estimation - Window Method

- Widely used in the industry
- Uses faults rather than defects
- Wafer maps that show the location of functioning and failing chips are analyzed using overlays with grids (also called windows)
- These windows contain some chip multiples (e.g., one, two, and four) and the empirical and theoretical yield for each such multiple is calculated
- Values for the parameters l , a , and Y_0 are then determined by means of curve fitting