UNIVERSITY OF MASSACHUSETTS
Department of Electrical and Computer Engineering

Fault Tolerant Computing ECE655

Homework 5

1. You have a task with execution time, T. You take N checkpoints, equally spaced through the lifetime of that task. The overhead for each checkpoint is T_{ov} and $T_{lt} = T_{ov}$. Given that during execution, the task is affected by a total of k point failures (i.e., failures from which the processor recovers in negligible time).

   (a) What is the maximum execution time of the task?

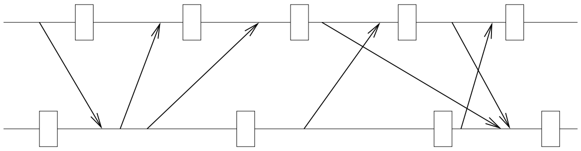
   (b) Find N such that this maximum execution time is minimized. It is fine to get a non-integer answer (say x): in practice, this will mean that you will pick the better of $\lfloor x \rfloor$ and $\lceil x \rceil$.

2. Solve the equation $e^{\lambda(T_{ex}+T_{ov})} = \frac{1}{1-\lambda T_{ex}}$ numerically and compare the calculated T_{ex}^{opt} to the value obtained in

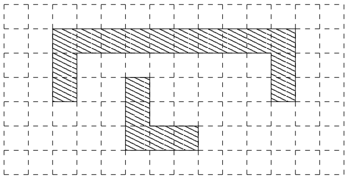
$$T_{ex}^{opt} = \sqrt{\frac{2T_{ov}}{\lambda} + 2T_{ov}\left(T_r + T_{lt} - \frac{T_{ov}}{2}\right)}$$

   for the simpler model. Assume $T_r = 0$ and $T_{lt} = T_{ov} = 0.1$. Vary λ from 10^{-7} to 10^{-2}.

3. Identify all the consistent recovery lines in the following execution of two concurrent processes:

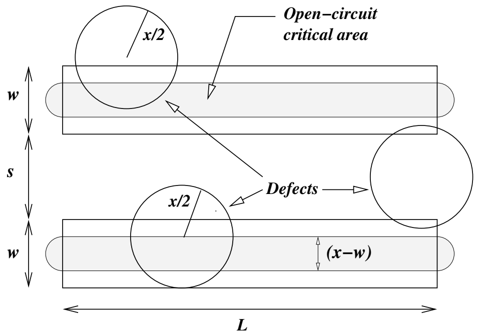


4. Use the polygon expansion technique to calculate approximately the critical area for circular short-circuit defects of diameter 3 for the 14×7 layout consisting of two conductors shown below.



5. (a) Derive an expression for the critical area $A_{miss}^{(c)}(x)$ of a circular missing-material defect with diameter x in the case of two conductors of length L, width w and separation s (as shown in the figure below). Ignore the non-linear terms, and note that

the expression differs for the three cases: $x < w$; $w \le x \le 2w{+}s$; and $2w{+}s < x \le x_M$.



(b) Find the average critical area $A^{(c)}_{miss}$ using the defect size distribution in the equation

$$f_d(x) \;=\; \begin{cases} kx^{-p} & \text{if } \; x_o \le x \le x_M \\ 0 & \text{otherwise} \end{cases}$$

with $p = 3$. For simplicity, assume $x_M = \infty$.

6. A chip with an area of 0.2 cm^2 (and no redundancy) is currently manufactured. This chip has a POF of $\theta = 0.6$ and an observed yield of $Y_1 = 0.87$. The manufacturer plans to fabricate a similar but larger chip, with an area of 0.3 cm^2, using the same wafer fabrication equipment. Assume that there is only one type of defects, and that the yield of both chips follows the Poisson model $Y = e^{-\theta A_{chip} d}$ with the same POF θ and the same defect density d.
   (a) Calculate the defect density d and the projected yield Y_2 of the second chip.
   (b) Let the area of the second chip be a variable A. Draw the graph of Y_2, the yield of the second chip, as a function of A (for A between 0 and 2).

7. A chip of area A_{chip} (without redundancy, and with one type of defects) is currently manufactured at a yield of $Y = 0.9$. The manufacturer is examining the possibility of designing and fabricating two larger chips with areas of $2A_{chip}$ and $4A_{chip}$. The designs and layouts of the new chips will be similar to those of the current chip (i.e., same θ), and the defect density d will remain the same.
   (a) Calculate the expected yields of the two new chips assuming a Poisson model.
   (b) Calculate the expected yields of the two new chips assuming a Negative Binomial model with $\alpha = 1.5$.
   (c) Discuss the difference between the results of (a) and (b).