Sample Test

UNIVERSITY OF MASSACHUSETTS
Department of Electrical and Computer Engineering

ECE 568/668

Final Exam

Open book and notes - 2 hours.
Solve all five problems.
Write your answers in the provided space.
Show your work and clearly mark your final answer.
5. (19 points) Briefly explain your answer to the following questions. A correct answer with no explanation is worth only one point.
(a) (5 points) The SPARC architecture can be implemented with two to eight register windows for a total of 40 to 136 general-purpose registers. Explain how these registers are organized into overlapping windows in each of the following designs: 1) 40 registers to construct two windows. 2) 72 registers to construct four windows.
(b) (8 points) A certain computer system includes a cache unit which employs the FIFO replacement algorithm. It was found that the resulting hit rate is not sufficiently high. Mark the suggestions that can increase the hit rate and indicate whether you expect a small or large effect:

1) Increasing the page size without changing the overall cache size.
2) Increasing the size of the main memory.
3) Increasing the size of the cache unit.
4) Employing the LRU instead of the FIFO algorithm.

(c) (6 points) List four factors that can affect the accuracy of the results obtained through trace driven simulation of a computer system with a cache-main memory hierarchy.
2. (21 points) The following sequence of compound vector statements is to be executed on a Cray X-MP vector processor:

$$C(I) = A(I) + s \times B(I)$$
$$D(I) = s \times A(I) \times B(I)$$

where $A(I)$ and $B(I)$ are each 64-element vectors of floating-point numbers originally stored in memory and s is a floating-point scalar already loaded into the floating-point register $F0$. The resulting vectors $C(I)$ and $D(I)$ must be stored back into memory after the computation. Assume that each pipelined unit has a latency (start-up penalty) of 6 clock cycles and a throughput of 1 operation per clock cycle.
(a) (7 points) Write vector instructions (you may use DLXV instructions which are Cray-like instructions) in proper order to execute the above statements on a Cray X-MP processor with two vector-load pipes and one vector-store pipe which can be used simultaneously with the remaining functional pipelines (including a single FP add/subtract unit and a single FP multiply unit).
(b) (7 points) Calculate the overall execution time of the above program for maximally chained vector operations for executing the above statements in minimum time.

Operation	Start	Complete

(c) (7 points) Calculate the potential speedup of the above vector chaining operations over the chaining operations on the Cray 1, which has only one memory-access pipe but the same number of FP add and multiply units.

Operation	Start	Complete

3. (18 points) The silicon area requirement of three DLX processors is to be examined. **Model A:** The superscalar DLX issues one integer and one floating point instruction each clock cycle. **Model T:** Similar to the model A, this superscalar DLX also issues up to one integer and one floating point instruction each clock cycle, but includes hardware for the Tomasulo Algorithm. **Model V:** The vector version of DLX, DLXV. It includes support for chaining.
All three models have an instruction cache containing 4096 bytes using 16 byte blocks that uses direct mapping, a fully pipelined floating-point (FP) adder and a fully pipelined FP multiplier. The models A and T also have a 4096-byte data cache with 64 byte blocks that is also direct mapped. Here is the cost of each resource needed to construct the models in terms of silicon area units:

1 bit of static RAM	0.001	area units
1 bit of register	0.002	area units
64-bit pipelined floating point adder or multiplier	1	area unit
Vector control unit (not including registers)	2	area units
Tomasulo control unit	2	area units
Single Tomasulo reservation station	0.1	area units
Integer control unit and ALU (not including registers)	1	area unit
Cache controller (including address comparator and muxes but no RAM)	1	area unit

What is the cost of each model? Fill in the table below the rest of the categories and sum the silicon area of each model.

Model A		**Model T**		**Model V**	
Integer control & ALU	1	Integer control & ALU	1	Integer control & ALU	1
Integer regs $(32 \star 32 \star 0.002)$	2	Integer regs $(32 \star 32 \star 0.002)$	2	Integer regs $(32 \star 32 \star 0.002)$	2
Scalar FP regs $(16 \star 64 \star 0.002)$	2	Scalar FP regs $(16 \star 64 \star 0.002)$	2	Scalar FP regs $(16 \star 64 \star 0.002)$	2
FP adder + multiplier	2	FP adder + multiplier	2	FP adder + multiplier	2
Instruction cache control	1	Instruction cache control	1	Instruction cache control	1
Data cache control	1	Data cache control	1	—	–
—	–	Tomasulo control unit	2	Vector control unit	2
Total		Total		Total	

4. (22 points) Consider a computer system designed for a transaction processing environment. The application has the following characteristic:

size of disk space = transaction rate x 10^7 bytes.

Each transaction takes 250,000 instructions which include 2 IO operations. The system includes a 20 MIPS CPU costing \$50,000 and you have to decide on the type of disks to be purchased. You have two choices but all disks purchased *must* be of the same type:
Type 1: 300 MB disks each capable of 30 IOPS and each costing \$10,000.
Type 2: 150 MB disks each capable of 40 IOPS and each costing \$8,000.
(a) (11 points) Find the maximum transaction rate and the number of disks (of either type 1 or type 2) required to achieve this rate.
(b) (11 points) Define cost effectiveness to be:

$$\frac{(Cost_{CPU} \cdot Fraction_{CPU\ used}) + (0.5 \cdot Cost_{disks} \cdot Fraction_{disk\ bandwidth\ used}) + (0.5 \cdot Cost_{disks} \cdot Fraction_{disk\ space\ used})}{Cost_{CPU} + Cost_{disks}}$$

Find the cost effectiveness of the two possible configurations (using disks of either type 1 or type 2) and determine which type of disks is preferable.