

UNIVERSITY OF MASSACHUSETTS  
Department of Electrical and Computer Engineering

ECE 568

Fall semester

Test 2

Open textbook, lecture notes and homework assignments only	1	_____	(30 points)
(use of architecture related software tools is not allowed).	2	_____	(20 points)
Solve all four problems - you have 2 hours.	3	_____	(25 points)
Write your answers in the provided space.	4	_____	(25 points)
<b>Show your work</b> and clearly mark your final answer.	Total	_____	(100 points)

State and **justify** any assumptions that you use.

Student name : \_\_\_\_\_

1. A pipelined processor uses a delayed branch with a single delay slot to eliminate stalls due to branches. Data forwarding is implemented, however, if the result of a Load is needed by the next instruction, 2 stall cycles are required. If the result of a floating-point multiplication is needed by another floating-point operation, 1 stall cycle is required. No stall cycle is required between any two other instructions. The following code operates on the double-precision floating-point elements of two arrays,  $X = (x_1, x_2, \dots, x_n)$  and  $Y = (y_1, y_2, \dots, y_n)$ . The addresses of these arrays are contained in R1 and R2, respectively. Initially, R3 contains the number of elements  $n$ , and both F3 and F5 contain zero.

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loop: ld      F1, 0(R1)    ; load  $x_i$ 
      ld      F2, 0(R2)    ; load  $y_i$ 
      addd   F3, F3, F1    ; add to F3
      multd  F4, F3, F2    ;
      addd   F5, F5, F4    ; add to F5
      addi   R1, R1, #8    ; increment pointer to first array
      addi   R2, R2, #8    ; increment pointer to second array
      subi   R3, R3, #1    ; decrement counter
      bnez   R3, loop
      nop                    ; branch delay slot
```

- (a) (5 points) Write an expression for the calculation performed by the above loop.
- (b) (8 points) How many cycles does each iteration in the above code take?
- (c) (6 points) Rearrange the code (no unrolling) so that it will take the smallest number of cycles per iteration. What is now the number of cycles per iteration?
- (d) (6 points) Unroll the loop once and schedule the instructions to minimize the number of stalls. What is now the number of cycles per iteration?
- (e) (5 points) If you would unroll the loop four times, what would be the number of cycles per iteration? (You don't need to actually unroll the loop to answer this question).

2. A given processor has separate instruction and data cache units. Each cache unit is of size 8KBytes, has blocks of size 32 Bytes and is direct mapped. The processor has a base CPI of 1.8 assuming perfect caches (i.e., 100% hit ratio) and given that it takes one clock cycle to access each cache. This CPI is achieved for an instruction mix which includes 20% data access instructions with 25% of them being writes. The two cache units are physically addressed and the TLB operates in parallel to the caches and as a result does not slow down a cache hit. The data cache uses Write Through with No Allocate upon a write miss but does not have a write buffer. The miss rates are: 1% for the instruction cache and 4% for the data cache. Upon a miss the main memory is accessed and this memory can transfer 4 bytes per (CPU clock) cycle with a latency of 50 cycles.

- (a) (12 points) Compute the CPI with the non-perfect caches but an ideal TLB (100% hit ratio).

(b) (8 points) Compute the CPI assuming that the TLB takes 60 cycles on a TLB miss and 2% of the memory references are not found in the TLB.

(c) (Bonus 5 points) If you could modify one parameter of the above design so as to reduce the CPI which one would it be? Explain and estimate the resulting CPI.

3. State whether each of the following statements is true or false and briefly explain your answer. A correct answer with no explanation is worth only one point. A correct answer with an incorrect explanation is worth 0 points.

(a) (5 points) If two instructions being executed in a superscalar experience exceptions, the exception that occurred first will be serviced first.

(b) (5 points) The loop  $for (i = 0; i \leq 100; i = i+1) \{ A[2i] = B[i]+C[i]; B[2i+1] = A[2i+3]+C[i+1] \}$  can not be unrolled.

(c) (5 points) The number of entries in the Reorder Buffer must be the same as that in the Result Shift Register.

(d) (5 points) The LRU replacement algorithm is commonly implemented rather than the optimal replacement algorithm since the latter requires a more expensive implementation.

(e) (5 points) The CPI of a quad-issue superscalar is one quarter of the CPI of a comparable single-issue processor.

4. In a main memory - disk virtual storage system the page size is 1KByte and the LRU algorithm is used for page replacements. A given program has been allocated three page frames in the main memory and it makes the following 16 memory references when it starts executing (the addresses are given in decimal):

2400, 900, 3500, 2100, 700, 5000, 400, 2800, 1500, 5500, 1000, 4000, 800, 2500, 2000, 500.

(a) (10 points) Show the contents of the three page frames after each memory reference and calculate the hit ratio.


(b) (8 points) Repeat (a) for the FIFO replacement algorithm.


(c) (7 points) Repeat (a) for the optimal replacement algorithm.
