



University of
Massachusetts
Amherst

Engin112 – Lecture 32

Timing Analysis

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Recap from last lecture

- Latches and Flip-flops
- Sequential circuits
 - FSM
 - Mealy, Moore
- Today's lecture
 - Timing in digital logic
 - » Combinational logic
 - » Sequential logic

Delay in Logic Circuits

- Circuits do not respond instantaneously to input changes
- Predictable delay in transferring inputs to outputs
 - Propagation delay (t_p)
- Sequential circuits require a periodic clock
- Goal: analyze clock circuit to determine maximum clock frequency
 - Requires analysis of paths from flip-flop outputs to flip-flop inputs
- Even after inputs change, output signal of circuit maintains original output for short time
 - Contamination delay (t_c)

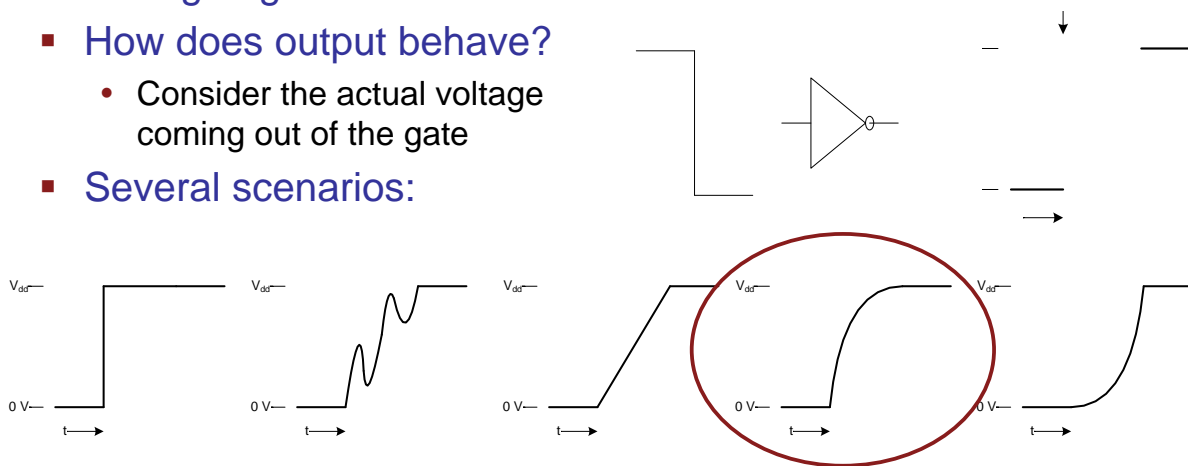
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Gate Output

- Falling edge on inverter:
- How does output behave?
 - Consider the actual voltage coming out of the gate
- Several scenarios:



- Why?
 - Output can be seen as RC circuit
 - » Capacitance (wires, transistors inside gates, etc.)
 - » Resistance (wires, inside gates, etc.)

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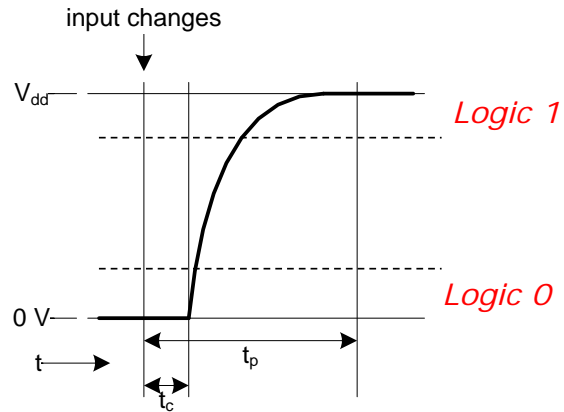
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Delays in Combinational Logic

- Gates have inherent delay
 - RC property determines delay
 - Gates cannot be made arbitrarily fast

- Delays in gates and circuits:

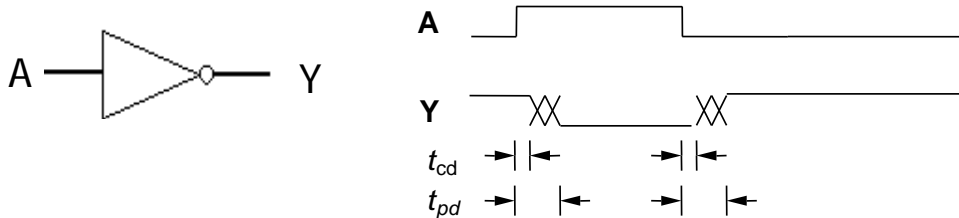
- Propagation delay (t_p)
 - » Delay between valid input and valid output
- Contamination delay (t_c)
 - » Delay between changed input and first change on output



- Both delays are important characteristics for circuits

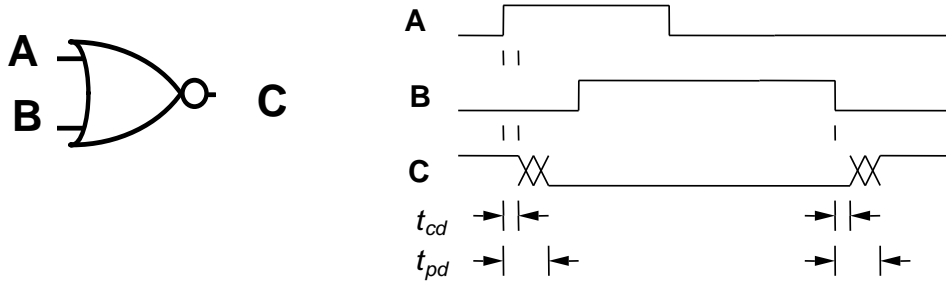
- Determine maximum clock rate

Combinational Logic Timing



- Combinational logic is made from electronic circuits
 - An input change takes time to propagate to the output
- The output remains unchanged for a time period equal to the contamination delay, t_{cd}
- The new output value is guaranteed to be valid (stable) after a time period equal to the propagation delay, t_{pd}

Combinational Logic Timing



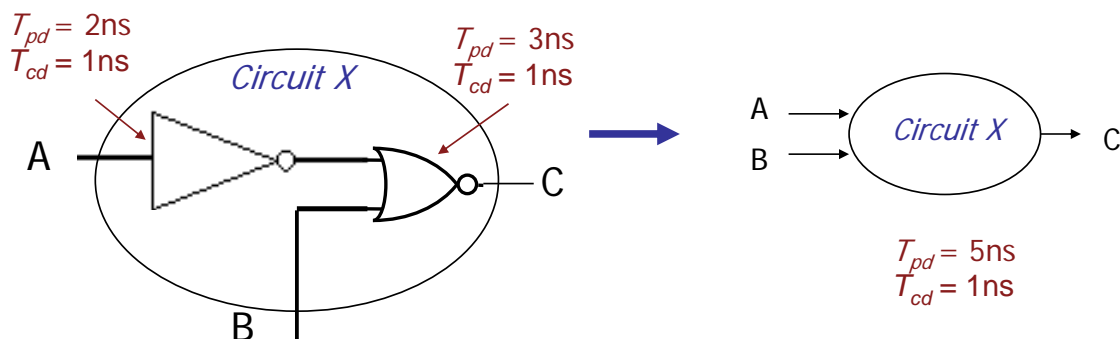
- The output is guaranteed to be stable with **old** value until the contamination delay
 - Unknown values shown in waveforms as Xs
- The output is guaranteed to be stable with the **new** value after the propagation delay

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Combinational Logic Timing



- Propagation delays are additive
 - Locate the **longest** combination of t_{pd}
- Contamination delays may not be additive
 - Locate the **shortest** path of t_{cd}
- Find propagation and contamination delay of new, combined circuit

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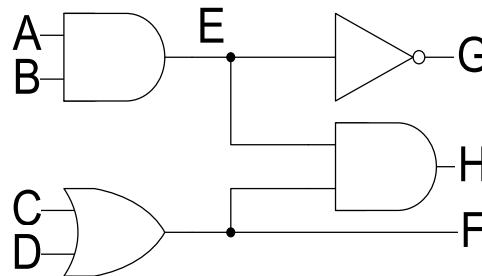
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Combinational Logic Delay - example

Gate delays:

- AND gate
 - » $t_c = 2\text{ns}$
 - » $t_p = 3\text{ns}$
- OR gate
 - » $t_c = 1.5\text{ns}$
 - » $t_p = 2.5\text{ns}$
- Inverter
 - » $t_c = 1\text{ns}$
 - » $t_p = 2\text{ns}$

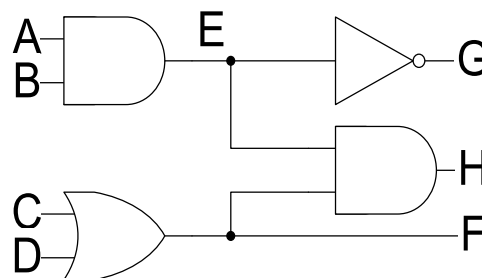


- What is the contamination and propagation delay of the circuit?

Contamination Delay - example

Consider every path

- AEG, BEG
- AEH, BEH
- CFH, DFH
- CF, DF



Contamination delay

- $t_c(\text{AEG}) = t_c(\text{BEG}) = 3\text{ns}$
- $t_c(\text{AEH}) = t_c(\text{BEH}) = 4\text{ns}$
- $t_c(\text{CFH}) = t_c(\text{DFH}) = 3.5\text{ns}$
- $t_c(\text{CF}) = t_c(\text{DF}) = 1.5\text{ns}$

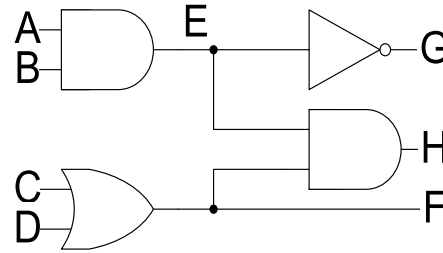
What is the contamination delay for this circuit?

- Shortest of all paths: $t_c = t_c(\text{CF}) = t_c(\text{DF}) = 1.5\text{ns}$

Propagation Delay - example

Propagation delay

- $t_p(\text{AEG}) = t_p(\text{BEG}) = 5\text{ns}$
- $t_p(\text{AEH}) = t_p(\text{BEH}) = 6\text{ns}$
- $t_p(\text{CFH}) = t_p(\text{CFH}) = 5.5\text{ns}$
- $t_p(\text{CF}) = t_p(\text{DF}) = 2.5\text{ns}$

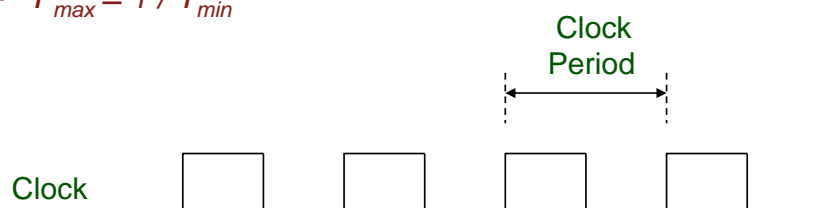


What is the propagation delay for the circuit?

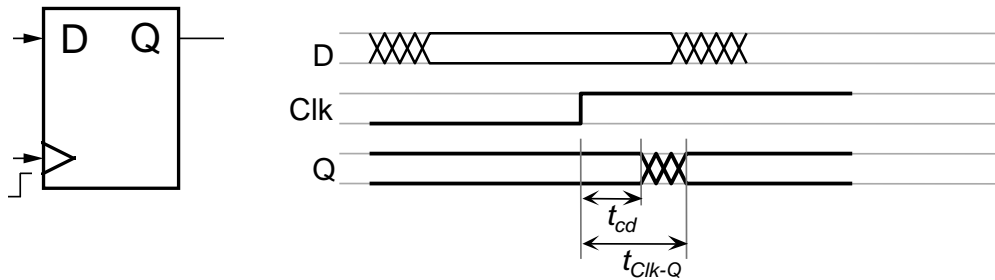
- Longest of all paths: $t_p = t_p(\text{AEH}) = t_p(\text{BEH}) = 6\text{ns}$

Sequential Circuits

- Sequential circuits can contain *both* combinational logic and edge-triggered flip flops
- A **clock** signal determines when data is stored in flip flops
- Goal: How fast can the circuit operate?
 - Minimum clock period: T_{min}
 - Maximum clock frequency: f_{max}
- Maximum clock frequency is the inverse of the minimum clock period
 - $F_{max} = 1 / T_{min}$



Clocked Device: Delays



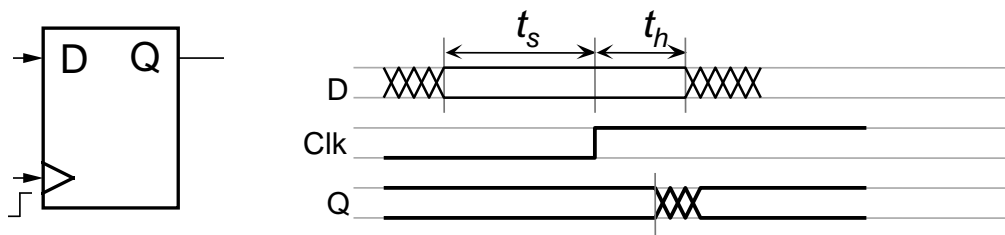
- Timing parameters for **clocked** devices are specified in relation to the **clock input** (rising edge)
- Output unchanged for a time period equal to the contamination delay, t_{cd} after the rising clock edge
- New output guaranteed valid after time equal to the propagation delay $Clk \rightarrow Q$, t_{clk-Q} (*why not t_{D-Q} ?*)
 - Follows rising clock edge

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Clocked Devices: Setup and Hold Times



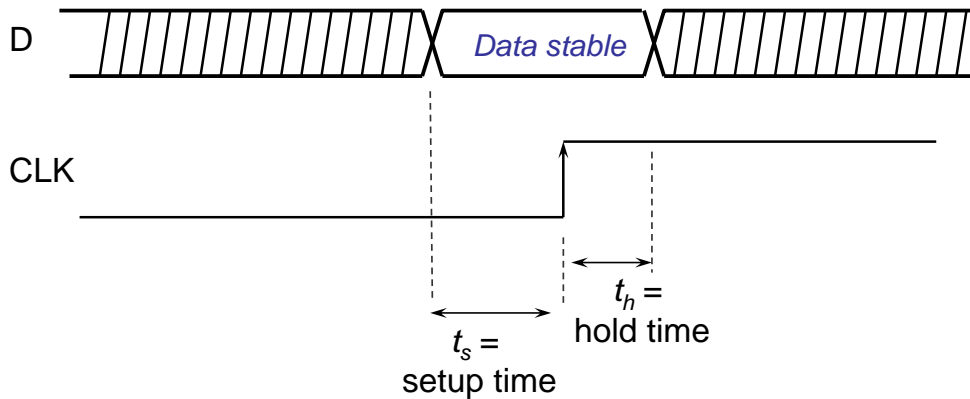
- Timing parameters for **clocked** devices are specified in relation to the **clock input** (rising edge)
- D input **must** be valid at least t_s (setup time) before the rising clock edge
- D input **must** be held steady t_h (hold time) after rising clock edge
- Setup and hold are input restrictions
 - Failure to meet restrictions causes circuit to operate incorrectly

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Edge-Triggered Flip Flop Timing



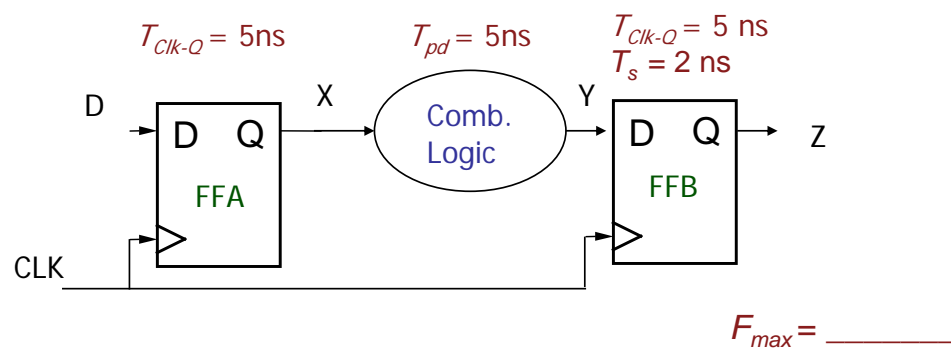
- The logic driving the flip flop must ensure that setup and hold are met
- Timing values (t_{cd} , t_{pd} , t_{clk-Q} , t_s , t_h)

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Analyzing Sequential Circuits



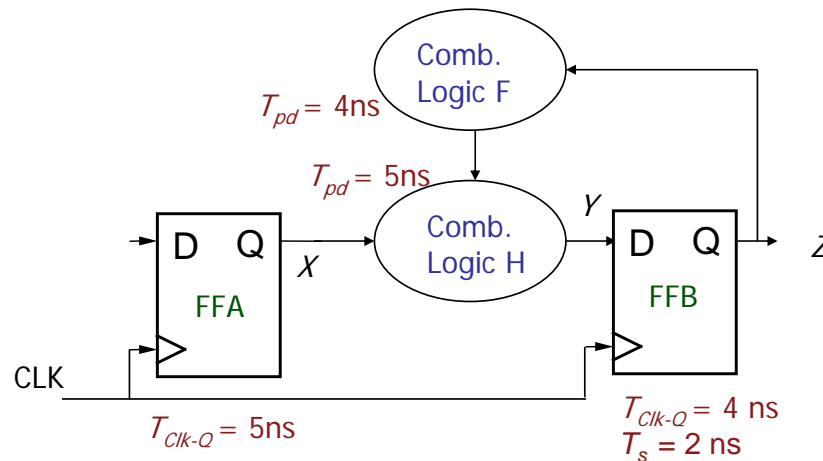
- What is the minimum time between rising clock edges?
 - $T_{min} = T_{CLK-Q} (FFA) + T_{pd} (G) + T_s (FFB)$
- Trace propagation delays from FFA to FFB
- Draw the waveforms, compute F_{max}

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Analyzing Sequential Circuits



- What is the minimum clock period (T_{min}) of this circuit?
 - Hint: evaluate all FF to FF paths
- Maximum clock frequency is $1/T_{min}$

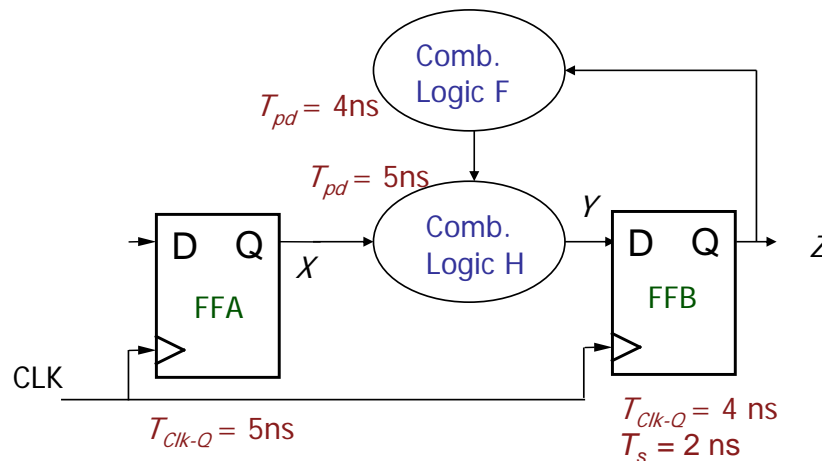
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Analyzing Sequential Circuits

$F_{max} = \underline{\hspace{2cm}}$



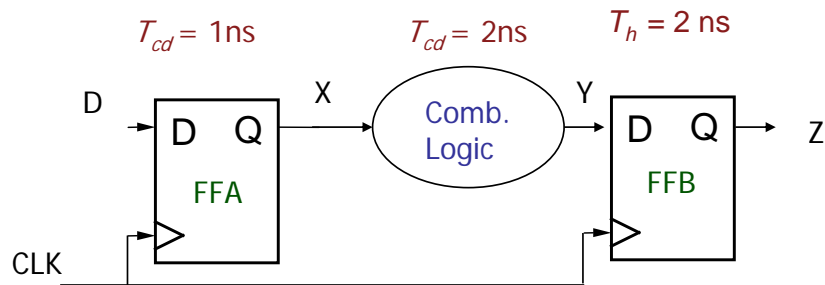
- Path FFA to FFB
 - $T_{clk-Q}(FFA) + T_{pd}(H) + T_s(FFB) = 5ns + 5ns + 2ns = 12ns$
- Path FFB to FFB
 - $T_{clk-Q}(FFB) + T_{pd}(F) + T_{pd}(H) + T_s(FFB) = 4ns + 4ns + 5ns + 2ns = 15ns$

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Hold Time Requirement



- One more issue: make sure that Y remains stable for hold time (T_h) after rising clock edge
- Remember:
 - contamination delay ensures that signal doesn't change for t_{cd}
- How long before first change arrives at Y ?
 - $T_{cd}(FFA) + T_{cd}(G) > T_h$
 - $1\text{ns} + 2\text{ns} > 2\text{ns}$

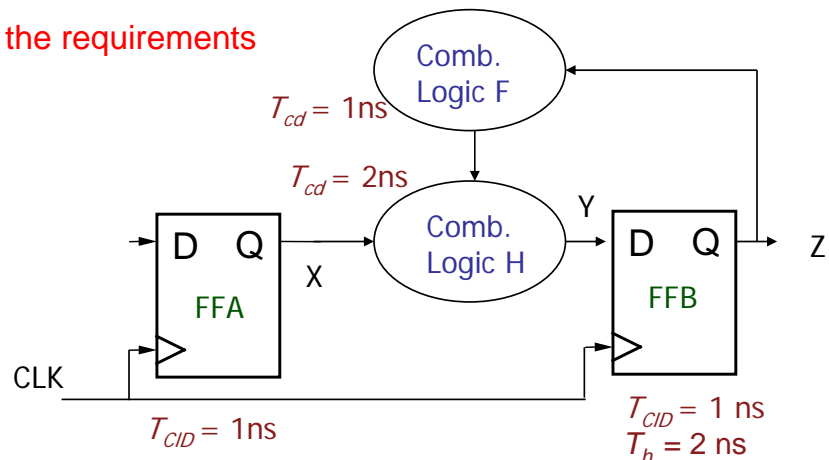
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Hold Time Requirement

All paths must satisfy the requirements



- Path FFA to FFB
 - $T_{CD}(FFA) + T_{CD}(H) > T_h(FFB)$
 $1\text{ ns} + 2\text{ns} > 2\text{ns}$
- Path FFB to FFB
 - $T_{CD}(FFB) + T_{CD}(F) + T_{cd}(H) > T_h(FFB)$
 $1\text{ns} + 1\text{ns} + 2\text{ns} > 2\text{ns}$

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Summary

- Maximum clock frequency is a fundamental parameter in sequential computer systems
- Possible to determine clock frequency from propagation delays and setup time
- The longest path **determines** the clock frequency
- All flip-flop to flip-flop paths must be checked
- Hold times are satisfied by examining contamination delays
- The **shortest** contamination delay path determines if hold times are met
- Check handout (pdf file) for more details and examples.