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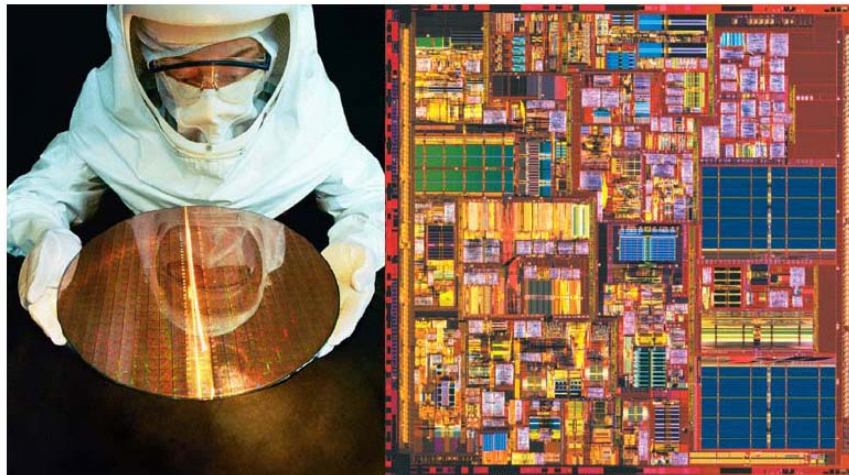
Engin112 – Lecture16

CMOS Electronic Devices

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11/12/2011

Implementation of Logic Gates

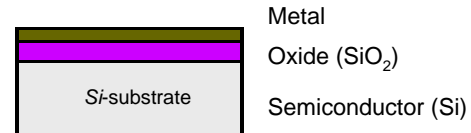
- Principles of operation of logic gates
 - Transistor as a switch
 - MOS transistor, CMOS process



- Reading assignment for this lecture
 - Mano, Chapter 10.7-10.8 (CMOS devices)

Device Physics - basics

- Current = flow of electrical charges
- Two types of charge carriers
 - Electrons
 - Holes
- Two types of semiconductors
 - n-type, rich in electrons
 - p-type, rich in holes
- MOS = metal, oxide, semiconductor structure
- MOS transistor = voltage-controlled switch
 - When control (gate) voltage = high (1), transistor is ON, conducts
 - When control (gate) voltage = low (0), transistor is OFF
- There are two types of MOS transistors
 - nMOS – conducting charges are *electrons*
 - pMOS – conducting charges are holes

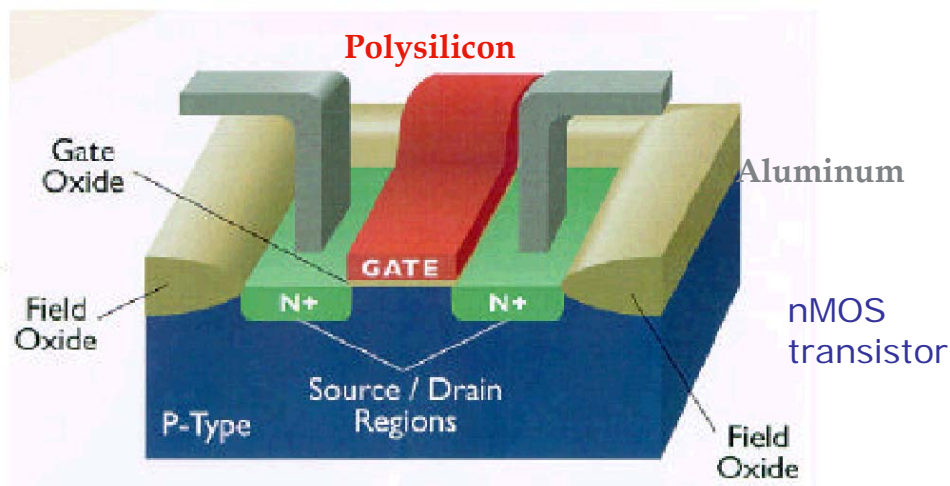


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The MOS Transistor



- nMOS transistor
 - electrons in the channel conduct current when Gate is ON (1)
- pMOS transistor
 - holes in the channel conduct current when Gate is OFF (0)

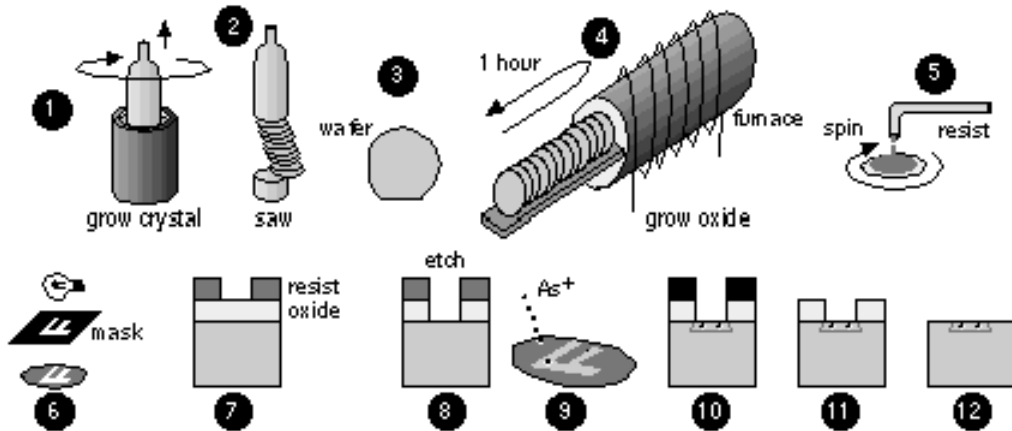
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The CMOS Process

- <http://www.youtube.com/watch?v=gBAKXvsaEiw&feature=related>
- <http://www.youtube.com/watch?v=wXVpQipeEh8&feature=related>

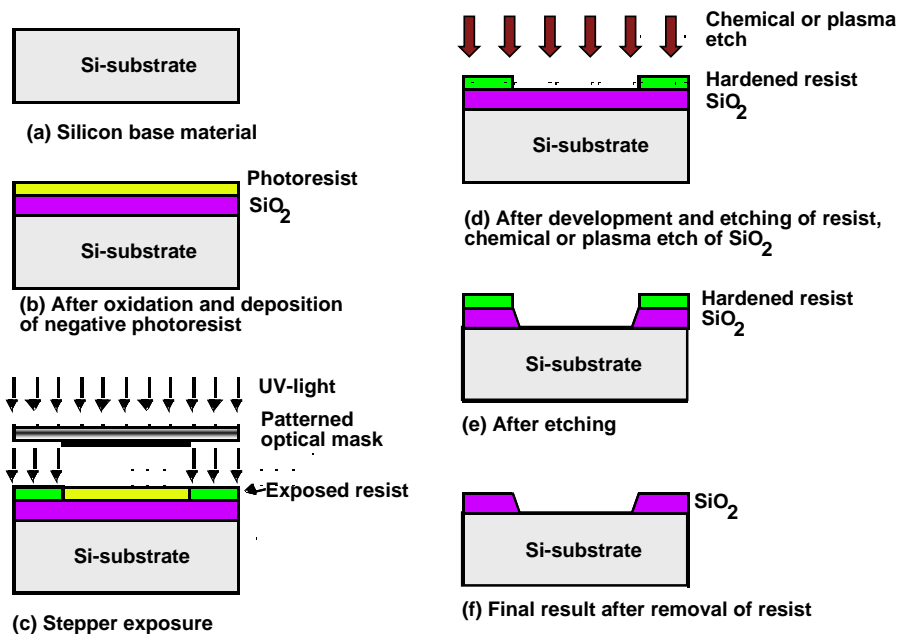


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Patterning of SiO₂



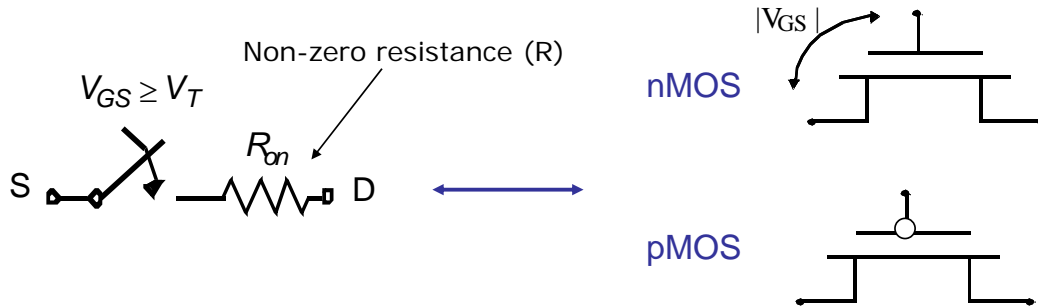
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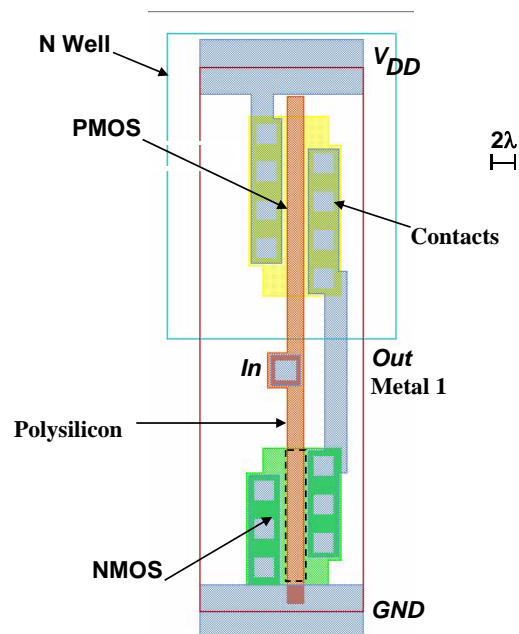
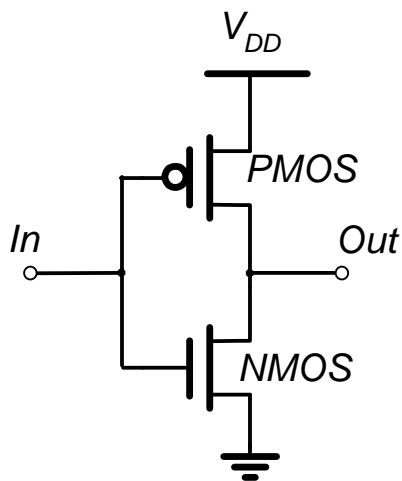
Transistor as a Switch

- We need a switch to turn the gate ON or OFF
- Switch implemented as MOS transistor

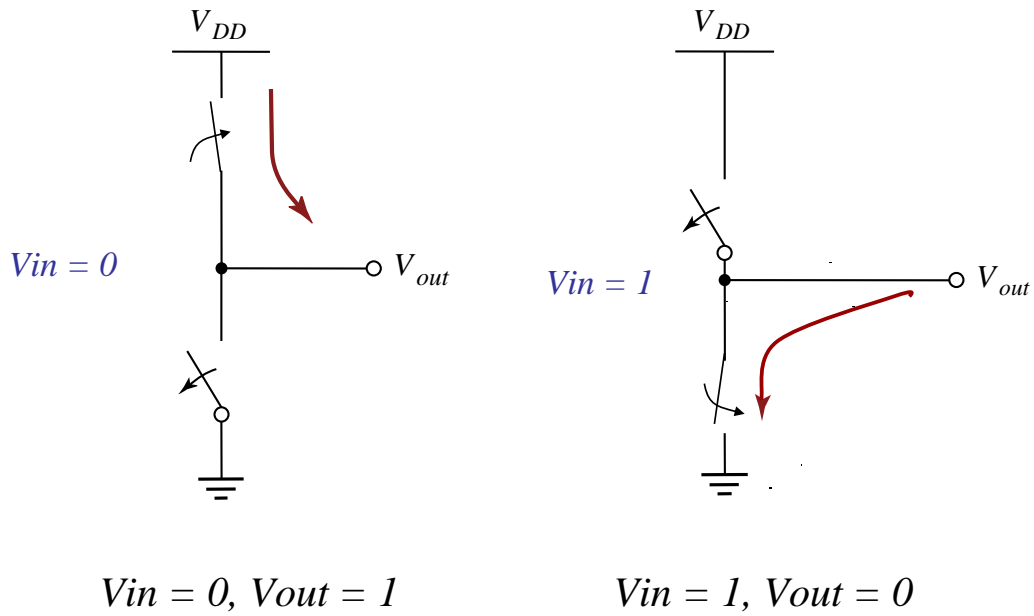


- V_T = threshold voltage, V_{GS} = gate-to-source voltage
 - V_{GS} must be greater than V_T to turn the transistor ON
- Two types of transistors/switches
 - *nMOS* – turns ON when gate voltage is logic 1, OFF when logic 0
 - *pMOS* – turns ON when gate voltage is logic 0, OFF when logic 1

CMOS Inverter



CMOS Inverter – Simplified Operation



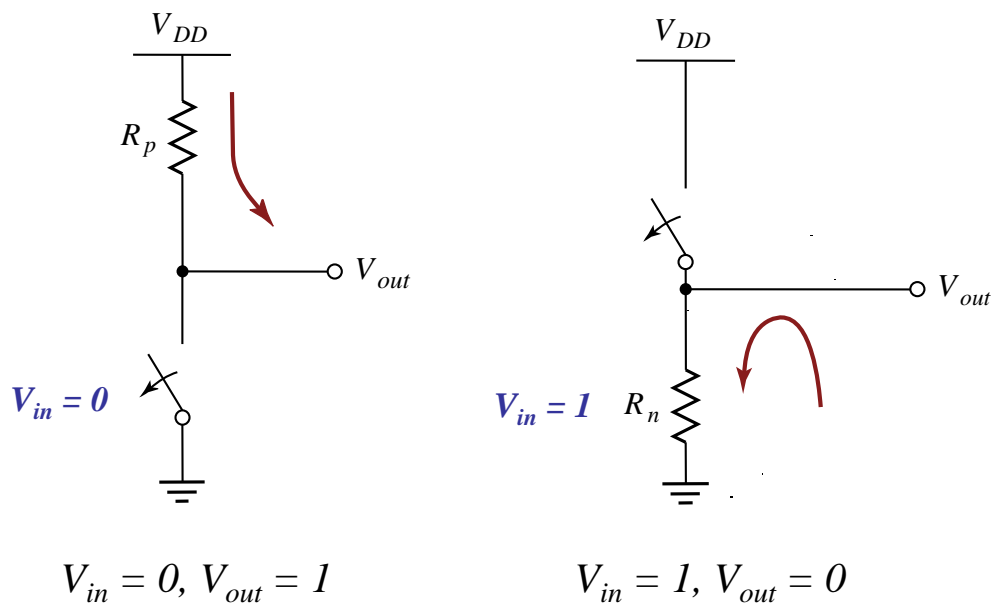
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CMOS Inverter - Operation

V_{dd} = power supply ($\sim 1.5V$)

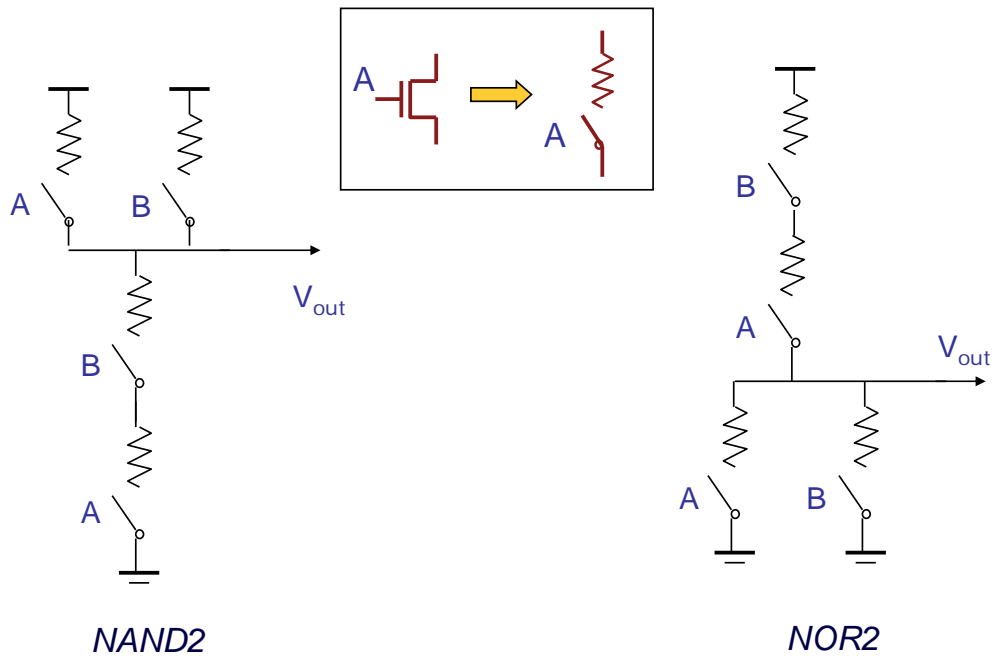


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CMOS NAND and NOR Gates

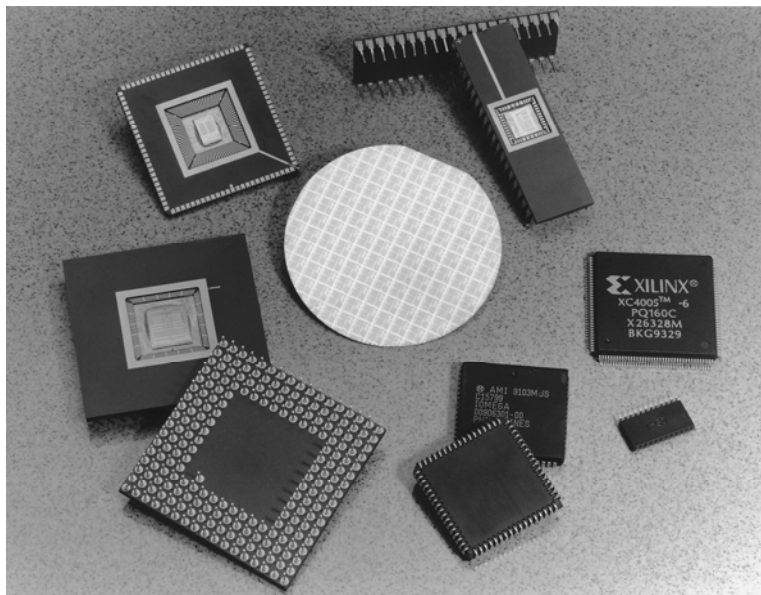


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Integrated Circuits

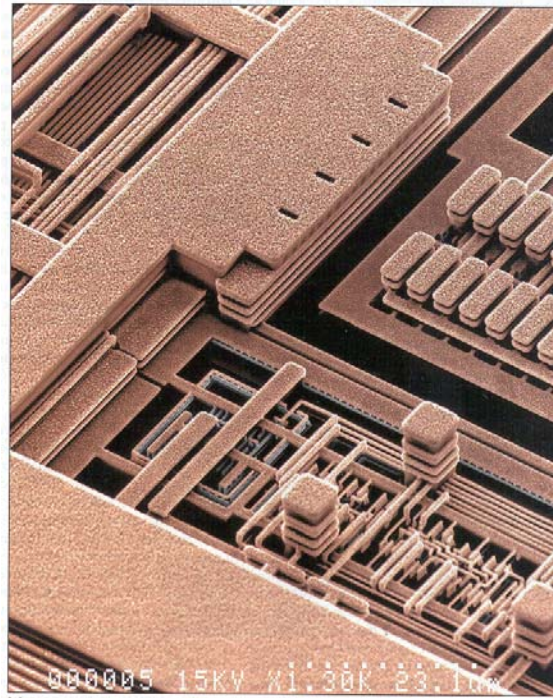
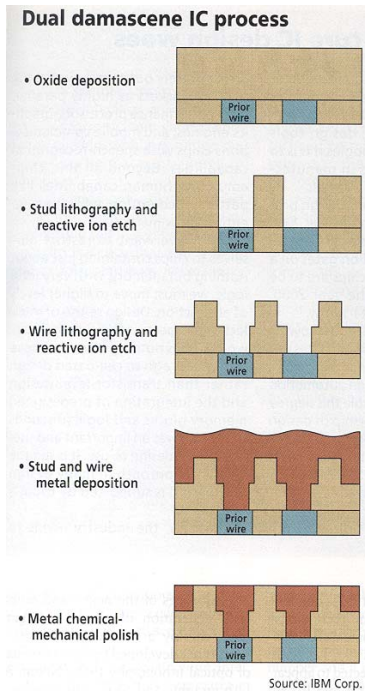


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Advanced Metallization

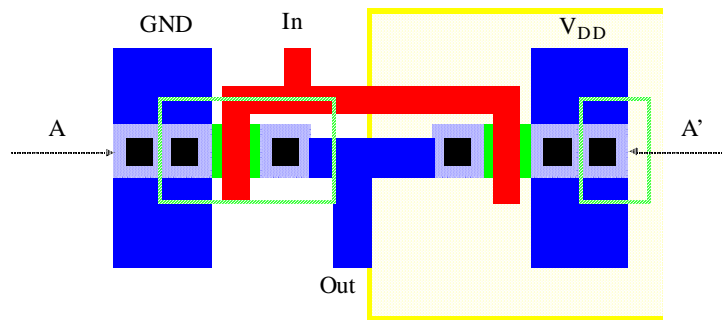


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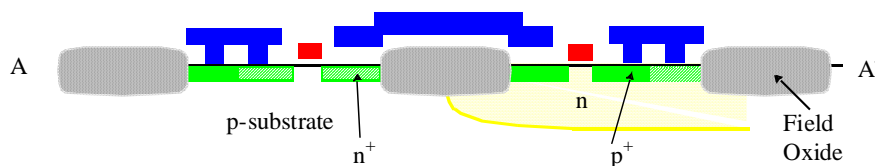
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CMOS Inverter Layout



(a) Layout



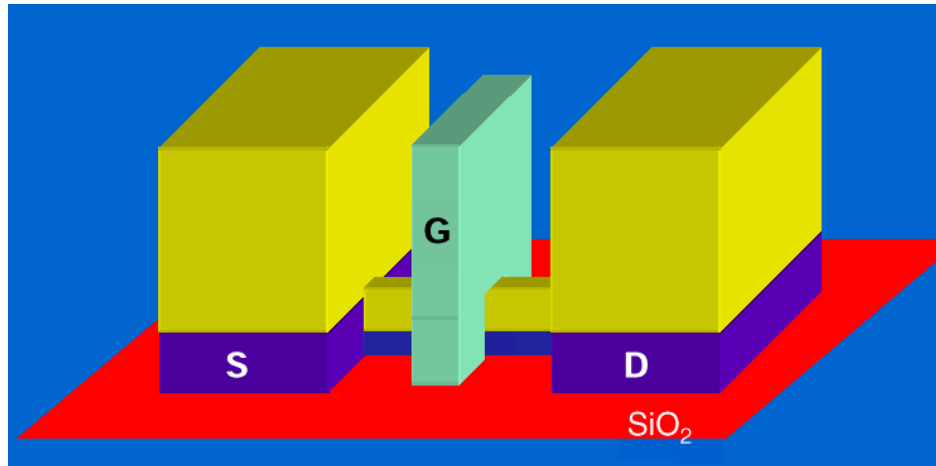
(b) Cross-Section along A-A'

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Perspectives



25 nm FINFET MOS transistor

Reading Assignment

- Read Mano 4.5 – 4.6 (Arithmetic circuits)