

Synthesis and Simulation with Altera's Quartus II software

This tutorial introduces you to Quartus II, a commercial software for synthesis and simulation of digital circuits, from Altera, one of the leading PLD/FPG manufacturers.

Quartus II software (for Windows) is available for free from the following website:

https://www.altera.com/support/software/download/sof-download_center.html

1 Creating the Design File

First you should create a design file. The design can be specified in any of the hardware description languages (HDL), such as Verilog, VHDL, or in a schematic format. The design in any of those formats can be created with Quartus using an appropriate editor.

- **Building the Design Schematic:** To create a schematic (block level, gate level, etc.), from the main **File** menu open **New file** to create a blank schematic on which to place your parts:
 - Click on **Device Design Files** tab
 - Select **Block Diagram/Schematic File** and Click OK.
 - You will now need to place schematic components (logic gates, input and output ports, wires, etc.). Click on the **AND gate symbol** on the sidebar (Below the big A) to bring up the Library of available parts. Click the + next to **primitives**, and then the + next to **logic** to open the Logic Gate Library. Select a gate you need for your design. Click OK.
 - Click to place the gate on the schematic. Repeat the procedure for other gates, as needed.
 - After placing the necessary gates, you will to wire them together. Select the **Orthogonal Node Tool**. Drag it from one pin to another to connect the inputs and outputs of the gates as needed.
 - Now you need to place the primary **inputs** and **outputs**. They can be found in the Primitives folder in the Device Library window under the **pin** subfolder.
 - Change the name of the input and output pins by double clicking on the generic pin_name. Type the name you need.
 - Optional: you can change the default state of the input pin by double-clicking on the VCC text of the pin. VCC means logic 1, GND means logic 0.
 - Save your design (it will be automatically given extension *.bdf).
- **Creating an HDL input file:** To create the design in Verilog HDL, in the main **File** menu open **New file**:
 - Click on **Device Design Files** tab
 - Chose item **Verilog HDL File** from the list

An editor window opens specifically for that format, where you will type the code for your design. Once you have created a file, make sure to save the file using Save As facility from the main File menu. To use VHDL instead of Verilog, follow the same procedure and choose VHDL file from the list.

2 Compiling and Synthesizing the Design

In order to compile and synthesize your design you need to open the design file and create a project for your design. For the Altera tools it is important that the name of the top module of your design has the same name as the file name containing the top module.

- From the main **File** menu choose **Open** to open your design file
- From the main **File** menu start **New Project Wizard** that will guide you in the creation of the project for your design. (If you already have an existing project, choose **Open Project** instead).
- The following information will be required to build the project file.
 - File name with the top module
 - Location of other modules/files, referenced by the top file
 - Device, such as Max, Stratix, Cyclon II, etc.
 - Optional: other, third party tools for simulation, verification, and synthesis to be used with this project.
- Once the project is created, you must compile your design. Depending on the type of simulation (functional or timing level) you will use, you will use different type of compilation.
 - For Functional Simulation, you only need to perform **Analysis & Synthesis** part of the compilation. This can be done by clicking on the middle violet compilation icon, second to the right from the STOP sign.
 - For full Timing Simulation, you must perform a complete compilation the design. Full compilation includes: initial design analysis and synthesis, fitting and assembling the design on the target device, and performing timing analysis. All of those steps are needed for timing analysis and for downloading the design onto the PLD device. Use the command **Start Compilation** from the main **Processing** menu or click on the Start Compilation icon (violet triangle next to the STOP sign) from the main menu.

3 Viewing Design after Compilation

This is a very useful feature that will allow you to view the design structure (netlist) and visually check your design. Several views, accessible from the main **Tools** menu are available.

- **RTL Viewer**, provides a hierarchical view of your design, from RTL down to gate-level, depending how your design was coded in HDL.
- **FSM Viewer**, gives a state transition diagram and table for designs written in a finite state machine format (with explicitly defined states)
- **Technology Mapped Viewer**, shows the design mapped onto lookup tables (LUTs)
- **Chip Viewer** provides physical view of the design.

4 Simulation

Two types of simulation are available: functional and timing. First you must create a simulation stimulus (input) for your simulation, called Vector Waveform File (VWF).

4.1 Creating Simulation Input (vector waveform file)

- In the main **File** menu open **New file**
 - click on **Other Files**
 - chose **Vector Waveform File** (VWF) item

A simulation window opens with two major fields: the left window is reserved for all the signals (input, output, registers, etc.) and the right window will show the actual waveforms.
- Before you start creating the waveform, you should define the *grid* in time units and the simulation time, called *end time*. To do that go to the **Edit** menu and choose **Grid** to set up the grid size, and **End Time** to define the simulation time. Pay attention to the units you use. The PLD devices available in the Quartus library run at 200 - 400MHz, so you can expect delays in the order of several nanoseconds.
- **Creating simulation waveforms**
 - Position the mouse in the left part of the window (reserved for signal names) and right-click there. Choose option **Insert Node** or Bus, and click on **Node Finder**. It will open a new window that will allow you to bring in the signals into the simulator. Use **Filter** to select the required signal types (e.g. **Pins**: all) and click on **List** to see the signals available for simulation. Select the signals you need in the **Nodes Found** window and move them to the **Selected Nodes** window using the > and >> buttons. When you close the window, the selected nodes will appear in the simulation window.
 - Select the signal you need (left click) and use the drawing tools and signal value assignment facilities (on the left part of the menu) to create a desired waveform.
 - Pay special attention to your clock signal. You can give it a periodic value by selecting (right click) its signal name, selecting the **Value** from the pull-down menu and then choosing the **Clock** option. A new window will open, which will allow you to specify the clock frequency and duty cycle.
- Make sure to save the input waveforms before performing simulation, typically under the same name as your design (with automatically given extension *.vwf*). If several versions of the simulation file are created, you have to tell simulator which *vwf* file to use. To do that, go to **Tools** menu, choose **Simulator Tool**, and provide the simulation file name in the Simulation input field.

4.2 Functional Simulation

To perform Functional Simulation, you must first run **Analysis & Synthesis** and set the simulation parameter to functional. You do not need to run the full compilation or timing analysis to perform functional simulation.

- From the **Main** menu, click on **Analysis & Synthesis** (middle violet triangle).
- Specify simulation settings by opening the **Processing** menu and choosing **Simulator Tool**. A window will open that will allow you to set the simulation mode. Set the simulation mode to **functional**. If you have already created the simulation input vector file you should provide the name of that file. This is a convenient feature if the same simulation input is shared among several designs (projects).
- (An alternative way to set the simulation parameters is to go to **Assignments** menu, then **Settings**, and choose **Simulator Settings**, which will open the same window. This path will allow you to set parameters for all the tools.)
- **Running the simulation** (common to both types of simulation)
 - Click on the simulation icon (blue waveform) from the main menu to start the simulation. (Alternatively, choose the **Start Simulation** option from the **Processing** menu). If you need to change the simulation parameters (grid size, end time, simulation file, etc.) go to the respective assignment menus as described above.
 - View the simulation results in the **Simulation Report**, automatically created in the main simulation window. If you want to make changes to the input waveform, do it on the original input simulation waveform (your *file.vwf*), not on the simulation result waveform.

4.3 Timing Simulation

To perform Timing Simulation, you must first fully compile and synthesize the design using one of the target devices (FPGA, PLD) from the Quartus II device library. The library is presented to you when you first create the Project. (You can change the device by opening the **Assignments** menu and then choosing the **Device** menu, if needed.) Only when the design is fully mapped on the target device will the software compute the actual delays of logic blocks and interconnect wires.

- Make sure to set the simulation mode to timing. From the **Tools** menu choose **Simulator Tool**. In the window that will open, set the simulation mode to **timing**.
- Running the simulation: same as in functional mode (refer to Section 4.2)

4.4 Advanced Features

- You can also set Simulation Breakpoints: go to **Processing** menu, then **Simulation Debug** menu and click on **Breakpoints**. A new window will open that will help you set up the breakpoints in your simulation.
- Quartus II allows you to compare the simulation results to a reference file, should you have one. To do that, go to the **View** menu and choose Compare to **Waveforms in File**.

5 Online Tutorials and Help

Additional information on the different tools and options of Quartus II is available using the **Help** menu and the embedded **Tutorial**.