ENGIN 112
Final Exam
Fall 2010

Prof. Ciesielski and Prof. Anderson

Name: ____

ID Number: ____

	Maximum	Achieved
Question 1	20	
Question 2	18	
Question 3	18	
Question 4	20	
Question 5	16	
Question 6	8	
Total	100	

This exam is <u>closed book, closed notes, open minds</u>. No calculators or other electronic devices allowed. Be concise, but show your work. Write legibly! Unreadable answers will not be graded.

Time: 120 minutes.

Question 1 (20 points): Give concise but complete answers to the following questions:

a) (2 pts) How many words can be stored in a random access memory with a word size of 16 bits and a total capacity of 4096 bits and how many address lines are needed to address this SRAM?

Words: ______________________

Address lines: ____________________

b) (2 points) For a random access memory with 256 words, what size decoder is necessary if:

Conventional decoding is used? One decoder of size ______________________

Coincident decoding is used? Two decoders of size ___________________ each.

c) (2 points) How many D flip-flops are needed to implement an FSM with five states:

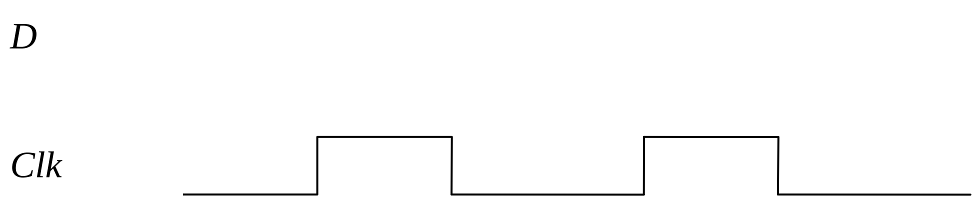
Mealy FSM : _________

Moore FSM: _________

d) (2 pts) Is this a Mealy or a Moore FSM ?

Label the diagram with present state (PS) and next state (NS) labels.

e) (2 pts) Illustrate the setup T_s and hold T_h times with a waveform for input signal *D* relative to the clock signal *Clk* assuming negative edge triggered clock.



f) (2 pts) What is the essential difference between a synchronous and asynchronous counter?

Asynchronous counter:

Synchronous counter:

g) (2 pts) Name which planes are programmable in the following programmable logic devices and write what these acronyms stand for.

PAL (means: ________________________________) :

PLA (means: ________________________________) :

ROM (means: _______________________________) :

h) (2 pts) Define the following terms and give examples of each for a 3-input function $F(a,b,c)$.

Minterm:

Product term:

Maxterm:

i) (2 points) Draw a block-level diagram of a 4-bit shifter that shifts to the left.

j) (2 points) Sketch a symbol for a multiplexer (MUX) with 5 inputs, clearly marking all inputs and output(s). How many select lines does this MUX need?

k) (**Extra Credit**, 2 points) Who invented Boolean logic and when (in which century)?

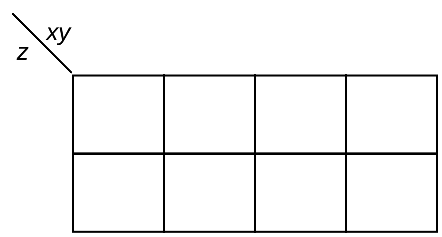
l) **Question 2** (18 points): Answer the following questions regarding the optimization of Boolean functions and their hardware implementation using standard combinational logic components.

Consider the logic function $F(x,y,z) = xy + yz' + xz + x'yz$

a) (4 points) Represent the function as a sum of minterms:

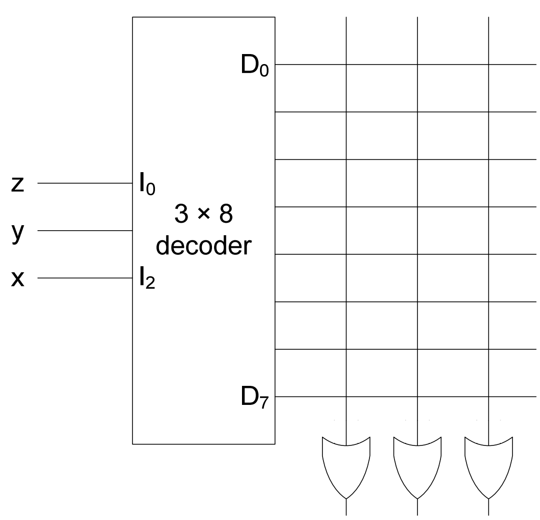
$F(x,y,z) = \Sigma$ ____

b) (4 points) Use a three-variable K-map to obtain minimum sum of product form for *F*:

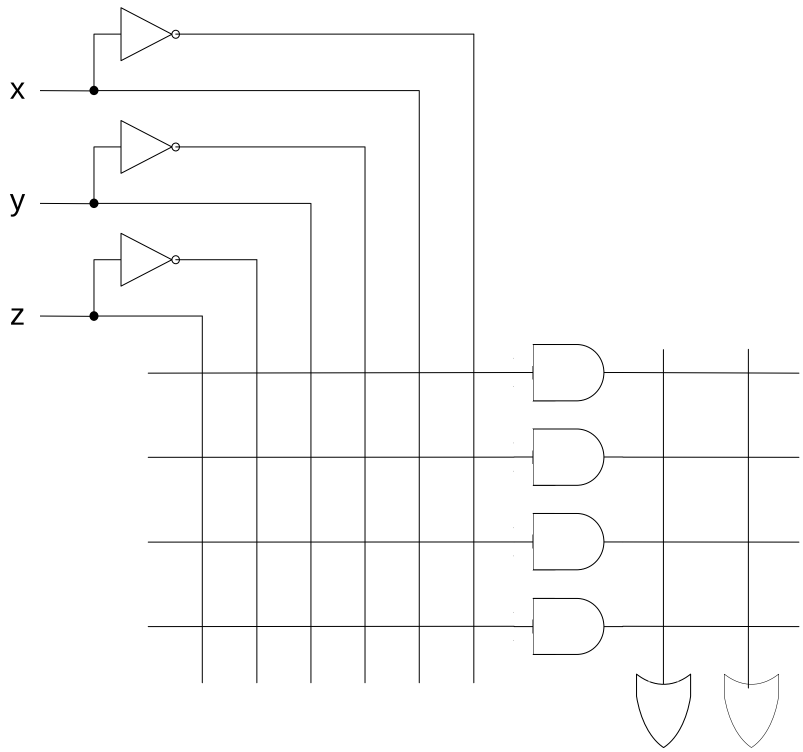


Minimized $F(x,y,z) =$ ____

c) (5 points) Implement function *F* with the ROM. Label all the necessary connections and fuses. Unused outputs should be left unlabeled.



d) (5 points) Implement the function *F* using a PLA. Unused product terms and outputs should be left unlabeled.

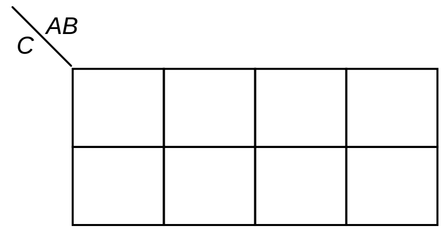


Question 3 (18 points):

Consider the Boolean function

G(A,B,C) = ABC +A'B'C + A'BC + ABC'.

a) (4 points) Derive the Karnaugh map and minimize *G(A,B,C)*.



G = ____________________________________

Now, answer the following assuming contamination delays t_c and propagation delays t_p of:

- t_c(NOT) = 1 ns t_p(NOT) = 2 ns
- t_c(AND) = 3 ns t_p(AND) = 4 ns
- t_c(OR) = 3.5 ns t_p(OR) = 4.5 ns
- t_c(NAND) = 2 ns t_p(NAND) = 3 ns

b) (7 points) - Draw the circuit diagram that implements the minimized form of *G* from part (a) using only *AND gates, OR gates, and inverters*. Generate complemented forms of any inputs that are required. Compute the contamination delay and propagation delay of the full circuit.

t_c(G) = ____________________ ns t_p(G) = ____________________ ns

c) (7 points) Redraw the circuit of part (b) using *only NAND gates and inverters*. Generate complemented forms of any inputs that are required. Compute the contamination delay and propagation delay of the full circuit.

$t_c(G)$ = ______________________ ns $t_p(G)$ = ______________________ ns

Question 4 (20 points):

Design a sequential circuit (electronic compass) with a single input *T* and outputs *A* and *B* that behaves as follows. Input *T* indicates the direction the person is turning:

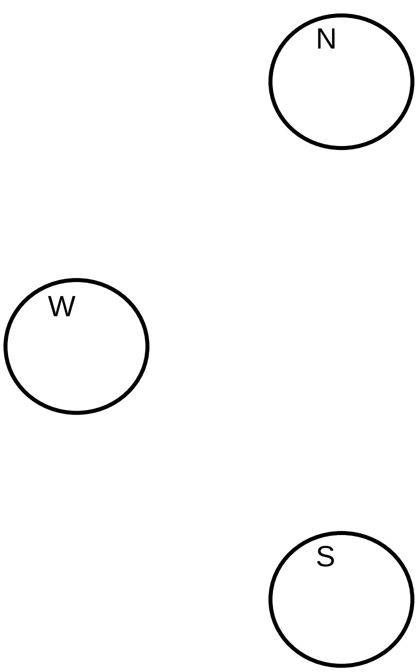
- *T* = 0 if turning 90 degrees to the right, and
- *T* = 1 if turning 90 degrees to the left.

The outputs indicate the binary code of the direction the person is facing after the turn:

- North: *A B = 0 0,*
- East: *A B = 0 1,*
- South: *A B = 1 0,*
- West: *A B = 1 1.*

Implement this circuit as a finite state machine with four states, N, E, S, W, (for North, East, South and West). Specifically solve the following problems:

a) Draw a state diagram for the circuit implemented as a Moore FSM. Label the states accordingly and show the output values and state transitions. (8 points)



b) Show the state table for this machine, encoding the states using state bits S_0 and S_1 as

North: $S_1S_0 = 00$ South: $S_1S_0 = 01$
East: $S_1S_0 = 10$ West: $S_1S_0 = 11$.

Label the table columns! (8 points)

T						

c) Determine the simplified functions for the signals *A* and *B* that must be generated by the output logic for this machine. (4 points)

Question 5 (16 points): Answer the following question regarding registers and sequential circuits.

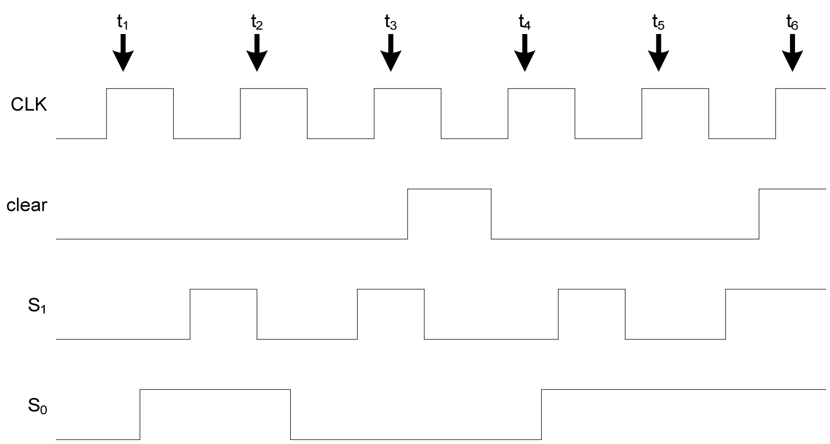
a) (8 points) Consider a universal shift register with the functionality shown in the table below:

Mode control		Register operation
S_1	S_0	
0	0	Parallel Load
0	1	Shift left
1	0	Shift right
1	1	No Change

The registers resets asynchronously to all 0's when *clear* is set to *clear*=1.
All other functions are positive edge triggered. Assume the following inputs:

- Parallel inputs: I_3=0 (left-most bit), I_2=1, I_1=0, I_0=1 (right-most bit)
- Serial input for right-shift = 0
- Serial input for left-shift = 1

Assume that the register is initially loaded with all 1's. What is the register value for the instances in time, $t_1 \ldots t_6$, marked in the following timing diagram?



Register value at t_1 is

Register value at t_2 is

Register value at t_3 is

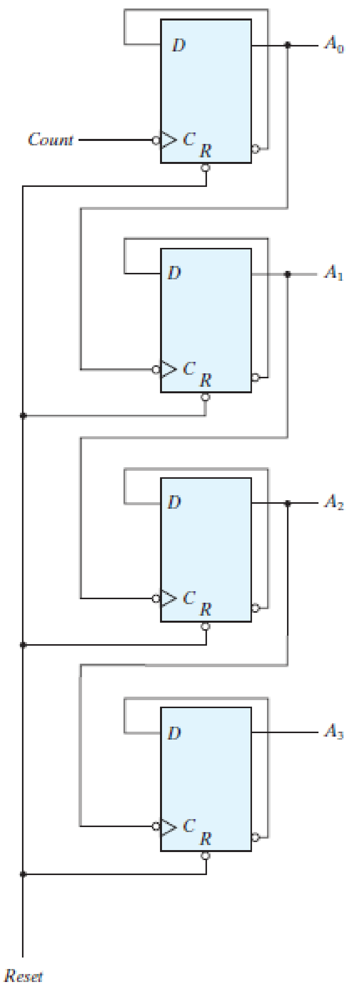
Register value at t_4 is

Register value at t_5 is

Register value at t_6 is

b) (8 points) Add a four-input NAND gate to the circuit diagram below, with

- the four NAND gate inputs connected to the signals A_3, A_2, A_1' and A_0.
- the NAND gate output connected to the "Reset" line.



A periodic clock signal is connected to the "Count" input. Assuming the flip-flop outputs are $A_3A_2A_1A_0$ = 1010 at some initial time when the clock is high, determine the circuit output…

- after the next negative clock edge: $A_3A_2A_1A_0$ = ____ ____ ____ ____
- after *two* negative clock edges: $A_3A_2A_1A_0$ = ____ ____ ____ ____
- after *three* negative clock edges: $A_3A_2A_1A_0$ = ____ ____ ____ ____
- after *four* negative clock edges: $A_3A_2A_1A_0$ = ____ ____ ____ ____
- after *five* negative clock edges: $A_3A_2A_1A_0$ = ____ ____ ____ ____

Your answers should assume that all transients occurring after the clock edge have settled down, i.e. that the output has stabilized to its final value for the clock cycle of interest.

Question 6 (8 points): Consider the RAM circuit on the following page, as well as the circuit diagram for the corresponding binary cells. Contents of the binary cells are shown for an initial time, when the memory is disabled (*EN*=0).

Determine the memory contents and circuit output after the inputs have been changed to….

a) Inputs: *EN* = 1 Read/Write = 1 Address = 11 Input Data = 1001

Memory Contents:

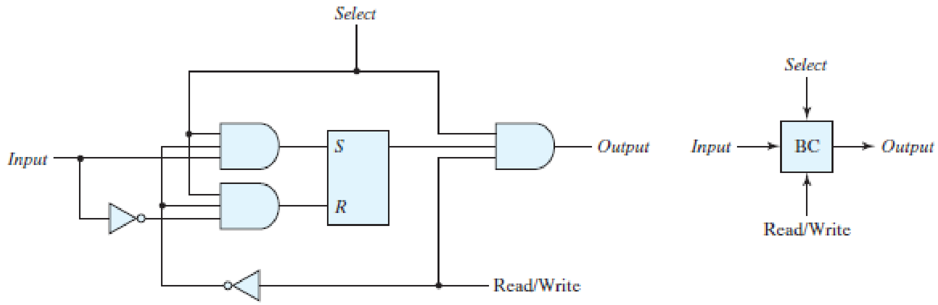
Output data = _____ _____ _____ _____

b) Inputs: *EN* = 1 Read/Write = 0 Address= 00 Input Data = 1001

Memory Contents:

Output data = _____ _____ _____ _____

Figures for Question 6



(a) Logic diagram (b) Block diagram