**SAMPLE PROBLEM SOLUTIONS – EXAM 2, FALL 2008**

**Question 1 (10 points)**:

Answer the following questions regarding decoders

a) Fill out the truth table for a 1-to-2 line decoder with input *I* and enable signal *En* (asserted high) and outputs $F_0$, $F_1$. ( 3 points)

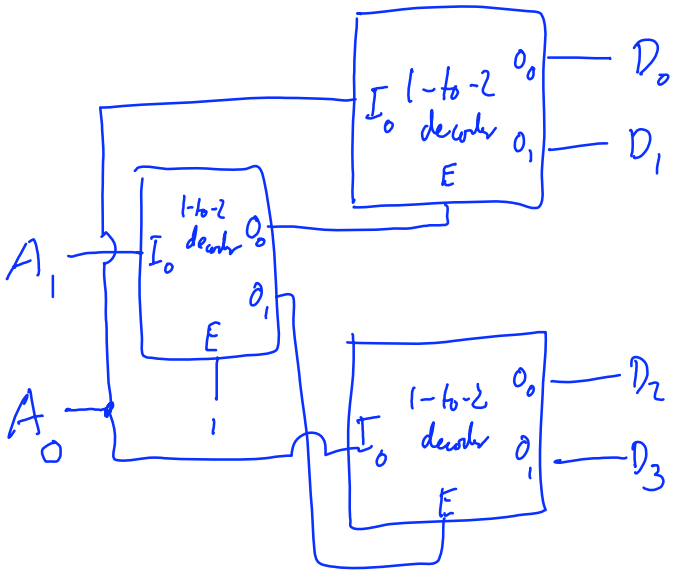
| *EN* | *I* | $F_0$ | $F_1$ |
|---|---|---|---|
| 0 | x | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

b) Draw the circuit (gate-level) diagram for this decoder. (2 points)

*It's OK to switch $F_0$ with $F_1$ in the table above and in the equation.*

$F_0 = EN\ I'$;  $F_1 = En\ I$

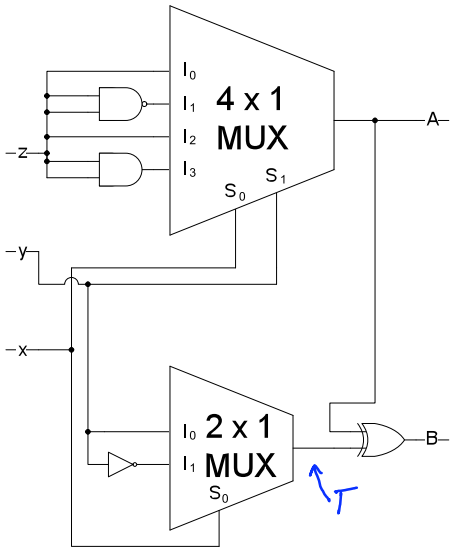
c) Using multiple 1-to-2-line decoders from part (a) design a 2-to-4-line decoder (with no enable) with inputs $A_0$, $A_1$ and outputs $D_0$, $D_1$, $D_2$, $D_3$. Show the block diagram only, with no internal circuit diagram of the decoders. (5 points)



**Question 2 (15 points)**:

Analyze the following combinational logic circuit.

a) Determine the outputs functions A and B as sums of minterms. You may use any process to determine the result, but show your work. (10 points)

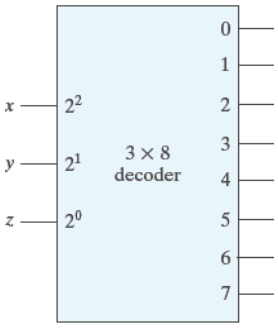



| *x* | *y* | *z* | *A* | *T* | *B* |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 |

$A(x,y,z) = \Sigma\ (\ 1, 2, 5, 6)$

$B(x,y,z) = \Sigma\ (\ 1, 3, 4, 6\ )$

b) Implement the same circuit using a decoder circuit and external logic gates. Show the block-level diagram of your design (5 points)




Connect the 3-to-8 line decoder's outputs (1,2,5,6) to an OR for A,
and outputs (1,3,4,6) to an OR for B.

**Question 3 (15 points)**:

Design a combinational circuit with three binary inputs: *H, S, I* and three binary outputs: *x, y, z*. Each input represents and item that a person may order at a fast food place:

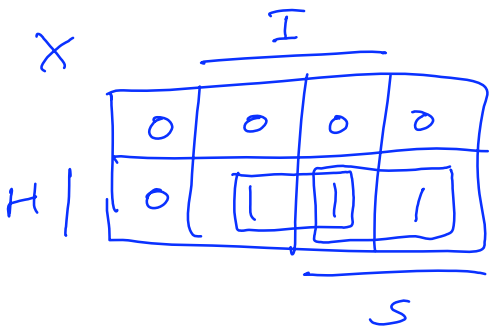
- *H* stands for hot dog, cost = $3
- *S* stands for soda, cost = $1
- *I* stands for ice cream, cost = $2

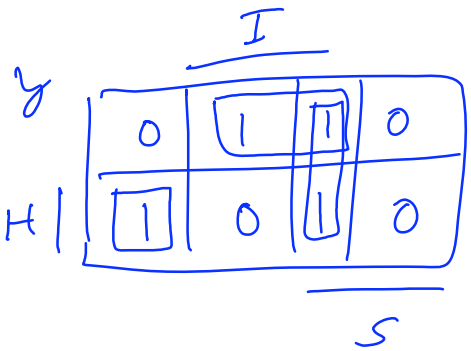
Each input can only be 0 or 1, which means that a customer can order each item only once (or none at all, for *H=0, S=0, I=0*).
The outputs *x,y,z* represent a 3-bit encoding $(xyz)_2$ of the total cost of the order. For example, for *H=1, S=0, I=0* (which evaluates to $3), the output should be *x=0, y=1, z=1*.

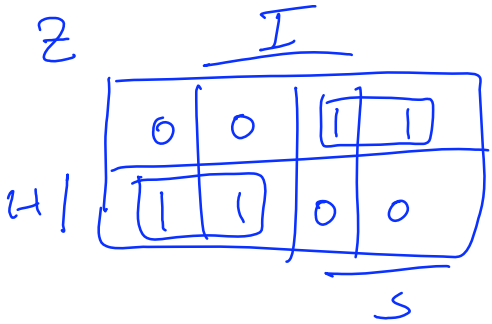
a) Show the truth table for this combinational circuit. (10 points)

| *H* | *S* | *I* | *x* | *y* | *z* | *cost* |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | $0 |
| 0 | 0 | 1 | 0 | 1 | 0 | $2 |
| 0 | 1 | 0 | 0 | 0 | 1 | $1 |
| 0 | 1 | 1 | 0 | 1 | 1 | $3 |
| 1 | 0 | 0 | 0 | 1 | 1 | $3 |
| 1 | 0 | 1 | 1 | 0 | 1 | $5 |
| 1 | 1 | 0 | 1 | 0 | 0 | $4 |
| 1 | 1 | 1 | 1 | 1 | 0 | $6 |

b) Determine the minimized functions *x, y, z* in a sum of products form. (5 points)



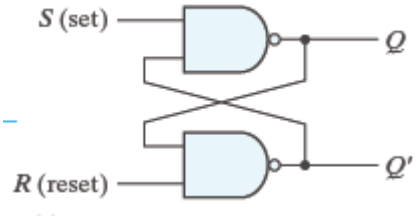

$x\,(H,S,I) = H\,I + H\,S$

$y\,(H,S,I) = H'I + S\,I + H\,S'I'$

$z\,(H,S,I) = H'S + H\,S'$

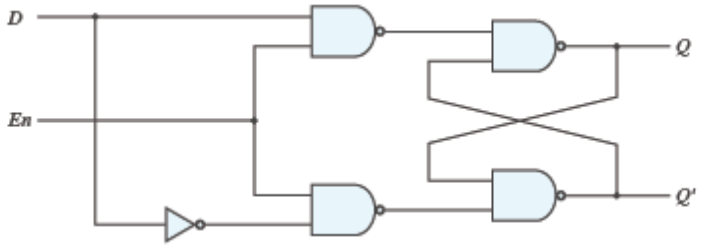
**Question 4 (10 points)**:
Answer the following questions regarding latches.

a) Draw the circuit of a NAND-based SR latch.
Fill in the function table below that shows the value of the outputs for different combinations of inputs S and R. (5 points)




| R | S | Q | Q' |
|---|---|---|---|
| 1 | 1 | $Q^{-1}$ | $Q'^{-1}$ |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 |

b) Draw the circuit of a D-latch using the SR latch designed in problem (a) (5 points).
(Hint: provide the D and EN inputs, properly wiring them to the S, R inputs)




| EN | D | Q |
|---|---|---|
| 0 | X | $Q^{-1}$ |
| 1 | 0 | 0 |
| 1 | 1 | 1 |