Sweep rate. Note that the presence of the Schmitt trigger section significantly degrades the synchronization performance of the flip-flop. The circuit of Fig. 1 was also tested by applying a negative-going marginal pulse to the set (S) input, after resetting, and the resulting output was the same as shown in Fig. 4.

The response of the Fig. 2 circuit is shown in Fig. 6. Here again the output can oscillate several times before settling. A TTL Schmitt trigger integrated circuit, the 7413, had been previously tested in a circuit somewhat like Fig. 2 to measure the probability that the Schmitt trigger was unresolved as a function of the time waited before sampling the output. The results of testing two packages indicate that 7413 Schmitt triggers in a circuit of the type shown in Fig. 2 will provide performance similar to that provided by crossed gates of the 7400 type.

The primary intent of this note is to challenge the belief still held by some logic designers that there is an electrical or logical circuit that will provide the synchronizer function, in a bounded time, with probability zero of a failure to synchronize. There are, of course, ways to improve synchronizer performance, but guaranteed resolution in a finite time is not possible. There are circuits that provide a zero failure rate in an unbounded time, but with a short average propagation time, for use in speed-independent, delay-insensitive asynchronous designs [4]-[6]. For clocked systems, a synchronizer design that uses a high-speed tunnel diode as the decision element in an ECL system has been reported to provide very good reliability with only an 11 ns propagation delay [6].

In closing, there is no great deal of theoretical and experimental evidence that a region of anomalous behavior exists for every device that has two stable states. The maturity of this topic is now such that papers making contrary claims without theoretical or experimental support should not be accepted for publication.

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Manuscript received September 11, 1978.
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Comments on “Multiple Fault Detection in Combinational Network”
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In the above paper, the authors have defined complete test, closed fault set, fault set graph, and undetected fault set as follows.

Definition 1—Complete Test (T): A complete test set detects any single fault in an irredundant network.

Definition 11—Closed Fault Set: A closed fault set is a set of faults such that each element in the set is masked by another element in the set when it is under test.

Definition 12—Fault Set Graph: A fault set graph is a graph with a vertex for each element in a set of multifaults and a directed edge between i and j if fault i masks fault j.

Manuscript received August 26, 1977. This work was supported by ONR Grant N00014-76-A048-643.
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Theorem 6: A set of faults will be UFS iff the set is a closed fault set.

The theorem has been proved in the above paper. It looks that the sufficient condition part of the theorem is not true always. For example, consider the circuit shown in Fig. 1. The set $T = (110, 011, 010, 101)$ is a single fault detection test set. Also, the masking condition $a/1 \rightarrow c/0 \rightarrow d/1 \rightarrow b/0 \rightarrow a/1$ is true for the circuit under test $T$. But the multiple fault $(a/1, b/0, c/0, d/1)$ which is a closed fault set by definition will be detected by either 110 or 011.

Apparently, the sufficient condition of the theorem is not valid. The authors have stated the following corollary.

Corollary 2: If a fault set graph contains only directed cycles, then the fault set is a UFS.

This corollary is derived from the sufficient condition part of Theorem 6. Hence, this corollary is not valid always.

Acknowledgment

The author wishes to thank Dr. T. R. N. Rao for his helpful comments.