ECE 571 - S'08 - LEC. 13

Recep CVD and continue on this topic.

CVD Metal deposition works well for Mo, Ta, Ti, W but NOT for Cu (see later about Cu).

A large group of processes are EPITAXY.

Basically grow a layer of a semiconductor (an "EPILAYER") on top of an existing substrate. EPI processes are basically some kind of CVD (poly-Si is a special case). Also Liquid-Phase epitaxy and Molecular beam epitaxy are used.

Basic process: Semiconductor grows:

\[ S = R \times N_S \]
Gas (tensile)
epi-
SiCl$_4$
layer

\[ \text{N} = \text{# molecules/cm}^2 \]

layer with density gradient

\[ J_g = \left( \frac{D_g}{\delta} \right) (N_g - N_s) \]

\[ D_g = \text{effective diffusion constant} \]

Growth rate \( \nu = \frac{J_s}{N} \) : In steady state \( J_g = J_s \rightarrow k_x N_s = \log (N_g - N_s) \)

So \( \nu = \frac{k_x \log N_g}{k_x + \log N} \)

\[ N_s = \frac{1}{\frac{k_x}{k_x + \log N}} \]

If \( k_x \gg \log \) — mass transfer limited

and \( \nu \sim \log \frac{N_g}{N} \)
If \( n_g \gg k_s \text{ - surface reaction limited and } \) 
\[ 2 \sim k_s \frac{n_g}{N} \]

See Fig. 6.10
Depends on the added gas. One must consider out-diffusion.

(Fig. 6.13)

Germanium can be grown from Getty ("germane").

One can also grow Si:Ge simultaneously and obtain an epilayer that is an SiGe alloy with a lattice constant between those for Si and Ge, and bandgap also in between:

- Si: \( E_g \sim 1.12 \text{ eV}, a \sim 5.43 \text{Å} \)
- Ge: \( E_g \sim 0.74 \text{ eV}, a \sim 5.64 \text{Å} \)
The layer of SiGe will be strained because it must adopt the same lattice constant as the Si substrate it is grown on but up to a certain critical thickness this is possible in 500nm/20nmGe.

A junction between two different semiconductors with different band gaps is called a heterojunction and is very commonly used especially in RF (wireless) semiconductor devices.

For example, SiGe bipolar transistors have a SiGe base layer—a "heterojunction bipolar transistor". It is often grown with ultra-high vacuum (UHV) CVD. Another example is SOS (Silicon on Sapphire) HBTs can also have a wide band emitter material such as Ga0.7Al0.3As with graded composition in the base and of close to GaAs and GaAs collector. See Figures.
III–V– semiconductor heterojunction devices are usually grown by molecular beam epitaxy—initiated 1970. MBE literally can deposit one atomic layer at a time.

GaAs and AlAs have the same lattice constant (and all alloys in between) so these epitaxial layers are NOT strained.

Similarly InP and Ga_{0.47}In_{0.53}As have the same lattice constant.

Other heterostructure devices are HEMTs (high-electron mobility transistors) and semiconductor lasers.

Often quantum wells are formed that guide electrons in heterostructure devices because of the different bandgaps (HEMTs, lasers).
MBE growth rates are very slow (10³ to 0.3 µm/minute) but are still used for RF and optoelectronic devices—not for silicon. The pressure is extremely low (∼10⁻¹³T). Earlier sources were by evaporation. Recent systems use gaseous sources.

Thin layers are also grown (faster!) by metal-organic CVD (MOCVD, also called OMVPE).

that the peak velocity for electrons in InGaAs is higher than for GaAs, see Figure 11.28. Recent simulation data, reproduced in this figure, show that a substantial advantage in peak velocity only occurs for $z \approx 0.5$, however.

Pseudomorphic HFETs have been developed during the last five years, and have been demonstrated to be superior to AlGaAs/GaAs HFETs in essentially all respects. In particular, $f_T$ and $f_{max}$ are higher, which means that PHFETs can be employed at much higher frequencies, and with lower noise figures. The process of decreasing the gate length appears to have paid off especially well for PHFETs, down to 0.1 micrometers, and perhaps even shorter. PHFETs have also been shown to be efficient power amplifiers.

As the gate length has been shortened, new phenomena have been uncovered which add to the models which have so far been established for HFETs.
Problem

Assume an effusion oven geometry of area \( A = 5 \, \text{cm}^2 \) and a distance \( L \) between the top of the oven and the gallium arsenide substrate of 10 cm. Calculate the MBE growth rate for the effusion oven filled with gallium arsenide at 900°C.

Solution

Upon heating gallium arsenide, the volatile arsenide vaporizes first, leaving a gallium-rich solution. Therefore, only the pressures marked Ga-rich in Fig. 3 are of interest. The pressure at 900°C is \( 5.5 \times 10^{-7} \, \text{atm} \) \( (4.2 \times 10^{-4} \, \text{Torr}) \) for gallium and \( 1.1 \times 10^{-5} \, \text{atm} \) \( (8.3 \times 10^{-3} \, \text{Torr}) \) for arsenic \( (\text{As}_2) \). The arrival rate can be obtained from the impingement rate (Eq. 56a) by multiplying it by \( A / \pi L^2 \):

\[
\text{Arrival rate} = 3.51 \times 10^{22} \left[ \frac{P_{\text{Torr}}}{\sqrt{MT}} \right] \left[ \frac{A}{\pi L^2} \right] \text{ molecules/cm}^2\text{-s}.
\]

The molecular weight \( M \) is 69.72 for Ga and 74.92\times 2 for \( \text{As}_2 \). Substituting values of \( P, M, \) and \( T \) (1173 K) into the above equation gives

\[
\text{Arrival rate} = 8.2 \times 10^{14}/\text{cm}^2\text{-s} \text{ for Ga}
\]
\[
= 1.1 \times 10^{16}/\text{cm}^2\text{-s} \text{ for As}_2
\]
Figure 12.15. Bandgaps for unstrained bulk $Si_{1-x}Ge_x$ alloys, as well as pseudomorphic $Si_{1-x}Ge_x$ layers. For the pseudomorphic case, the valence band splits into a heavy and a light hole band - both are shown. Reprinted from IYER, S.S., PATTON, G.L., STORK, M.C., MEYERSON, B.S., and HARAME, D.L. (1989). "Heterojunction Bipolar Transistors Using Si-Ge Alloys," IEEE Trans. Electron Devices, ED-36, 2043, ©1989 IEEE.

NOISE PROPERTIES OF HBTs

The noise model for an HBT is the same as for the BJT, i.e. the main sources of noise are resistive noise in the base, and shot noise in the emitter and collector currents, respectively. The base resistance of the HBT is lower due to the high doping, commensurate with the higher values for $f_{max}$. It is thus expected that HBTs, including SiGe/Si versions, should have reasonably low noise up to much higher frequencies than BJTs. The noise figure of HBTs at around 10 GHz presently is about 3 dB, which is not competitive with MESFETs and HFETs. The HBT noise figure is also expected to reach a "corner" frequency above which it will increase as $f^2$, whereas FET noise figures increase essentially linearly with $f$, according to the Fukui expression. Only a few measurements of HBT noise figures have been performed so far, and Figure 12.16 shows the trend of the data. With further development, one expects these values to decrease, of course, but it is also likely that FET noise figures will always stay lower.

Recombination often determines a value for $\beta_{max}$ which is smaller than that given by (12.26). Recombination is especially fast at the interfaces, if these contain defects. The geometry of the HBT favors a low total recombination rate, since most of the current proceeds from the emitter to the collector through the inside of the base, far from any interface. It is thus possible to achieve sufficiently high $\beta$ values. In a typical HBT, recombination in the emitter-base depletion layer, due to deep-level recombination centers, dominates.

The reference in the quotation from (Kroemer, 1982) at the beginning of this section to "an idea whose time has come", of course relates to the fact that growth and fabrication technologies in the decades following the initial proposal for using an emitter with a wider energy gap (Shockley, 1948), were not up to the task of realizing such a device. Kroemer (1957) had later analyzed these ideas in considerable detail. It was clear that III-V compounds were most promising. With the development of MBE and OMCVD growth methods, the 'time had come' to realize HBT devices,
Table 12.1.
Representative HBT epitaxial layer structure.

<table>
<thead>
<tr>
<th>COMPOSITION</th>
<th>THICKNESS (Å)</th>
<th>DOPING (cm⁻³)</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>$n^+ \text{ GaAs}$</td>
<td>750</td>
<td>$1 \times 10^{19}$</td>
<td>Cap</td>
</tr>
<tr>
<td>$n^- \text{ GaAs}$</td>
<td>1250</td>
<td>$5 \times 10^{17}$</td>
<td>Cap</td>
</tr>
<tr>
<td>$n^- \text{ Ga}_0.7\text{Al}_0.3\text{As}$</td>
<td>2500</td>
<td>$5 \times 10^{17}$</td>
<td>Emitter</td>
</tr>
<tr>
<td>$p^+ \text{ GaAs}$</td>
<td>500–1000</td>
<td>$5 \times 10^{18} - 1 \times 10^{20}$</td>
<td>Base</td>
</tr>
<tr>
<td>(or InGaAs)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$n^- \text{ GaAs}$</td>
<td>5000</td>
<td>$3 \times 10^{18}$</td>
<td>Collector</td>
</tr>
<tr>
<td>$n^+ \text{ GaAs}$</td>
<td>6000</td>
<td>$4 \times 10^{18}$</td>
<td>Sub-Collector</td>
</tr>
<tr>
<td>Semi-ins. GaAs</td>
<td>0.1–0.5 mm</td>
<td></td>
<td>Substrate</td>
</tr>
</tbody>
</table>


In other discussions of the HBT, we will find it convenient to directly make use of most of the formalism we have presented for BJTs above.

STRUCTURE AND I-V-CHARACTERISTICS OF HBTs

A representative structure of an HBT is illustrated in Figure 12.10 (Asbeck et al., 1989). The emitter contact is at the top of the entire device, while mesas are etched in order to contact the base and collector as closely as possible. Self
We have already discussed the importance of $f_T$ as an RF figure of merit but $f_{MAX}$ is also important as it is more strongly influenced by parasitic base resistance, which can influence noise figure as shown in (1), and collector-base capacitance which can influence the gain and linearity of RF amplifiers. $f_T$ and $f_{MAX}$ are related to basic device parameters by the commonly used equations

$$f_T = \frac{1}{2\pi \cdot \tau_f}$$

$$\tau_f = (C_{be} + C_{bc}) \cdot \left( R_e + \frac{kT}{qI_c} \right) + \frac{W_b^2}{2D_b} + \frac{W_c}{2v_s} + R_c \cdot C_{bc}$$

$$f_{MAX} = \sqrt{\frac{F_t}{8\pi \cdot R_b \cdot C_{bc}}}$$

where $\tau_f$ is forward transit time, $C_{be}$ is emitter-base capacitance, $C_{bc}$ is base-collector capacitance, $R_e$ is emitter series resistance, $W_b$ is vertical base width, $D_b$ is electron diffusivity in the base, $v_s$ is electron saturation velocity, $W_c$ is collector-base vertical depletion width, and $R_c$ is collector resistance.

Lithography advances with each new technology node enable lateral device scaling. In a bipolar device, there are several dimensions that can benefit from scaling as shown schematically in Fig. 4 including: the emitter width, the link base region, the selectively-implanted-collector (SIC) to extrinsic base separation, and the width of the base-collector island.

Fig. 4. Sketch of a SiGe NPN showing dimensions targeted for scaling with each generation marked by numbers 1 through 4 where: 1 is the emitter width, 2 is the link base region, 3 is the separation between SIC implant and the extrinsic base region, and 4 is the width of the base-collector island.

Fig. 5. (a) $f_T$ and (b) $f_{MAX}$ as a function of emitter size for emitter widths of 0.15–0.2 μm with $V_{bc} = 1$ V [3].
These measurements include 1) the well-documented difficulty in accurately 2) measuring data at relevant application frequencies, 3) internal impedance mismatch at low frequency, and 4) current and bias on noise. The S-parameter transmission coefficients for input, output, and mm-wave. The 2003 ITRS curve is shown as the solid line.

The limit is substantially at lower gate bias and circuit scaling may be offset as bias increases. As circuit scaling continues, RF noise increases along with gate leakage currents with the importance of substrate resistance and contamination that results from higher temperature. The RF noise issue is treated in the following the minimum value of the

$$f_T = \frac{1}{2\pi R_C} \ln (1.2) \left( G_M + 2G_D + 2G_S \right)$$

where the corner frequency has to be derived. The corner frequency is the point where the noise on the 1/f-noise amplitude is dominant over white noise. Thus, the corner frequency is a boundary for importance of circuit. The corner frequency for SiGe is approaching several 10s even when assuming constant technology scaling. This function is difficult to predict. This is because 1) the relatively large chip areas required to implement RF functions do not scale as fast as digital circuit density, 2) significant time is required to implement complex RF designs, and 3) noise issues