

Homework 7

1. **Problem:** (a) Consider an n-channel MOSFET with uniform channel doping with $N_A = 3 \times 10^{17} \text{ cm}^{-3}$ and having an oxide 10 nm thick. Calculate the sub-threshold slope at 300 K.
(b) Assume now that the Si-SiO₂ interface is not ideal, but there are interface traps with density $N_{it} = 10^{12} \text{ cm}^{-2} / \text{eV}$. What is the sub-threshold slope in this case?

Solution:

- (a) On lecture notes Part 3, the subthreshold slope is given by Eq. (280)

$$S = \frac{k_B T}{e} \ln(10) \left(1 + \frac{C_D}{C_{ox}}\right) \quad (1)$$

where $C_D = \frac{\epsilon_s}{W_{D,max}}$ and $W_{D,max}$ is the maximum depletion width defined by Eq. (221)

$$W_{D,max} = \left[\frac{4\epsilon_s k_B T \ln(N_A/N_i)}{e^2 N_A} \right]^{1/2} = 61.5 \text{ nm} \quad (2)$$

and

$$C_D = \frac{11.7 \times 8.854 \times 10^{-12} \text{ F/m}}{61.5 \times 10^{-9} \text{ m}} = 0.0017 \text{ F/m}^2, \quad (3)$$

and $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = 0.0034 \text{ F/m}^2$. Inputting the above values and finally we can get the sub-threshold slope $S = 0.0892$.

- (b) When the Si-SiO₂ interface is not ideal with an interface traps density $N_{it} = 10^{12} \text{ cm}^{-2}$, the subthreshold slope is calculated using Eq. (282)

$$S = \frac{k_B T}{e} \ln(10) \left(1 + \frac{C_D + C_{it}}{C_{ox}}\right) \quad (4)$$



where C_{it} is given by Eq. (226)

$$C_{it} = eN_{it} = 0.0016F/m^2, \quad (5)$$

therefore, the corresponding sub-threshold slope $S = 0.1172$. Clearly, the smaller the value of S , the better the transistor is as a switch. A small value of S means a small change in the input bias can modulate the output current considerably and thus less power consumption. Therefore, the $Si - SiO_2$ interface traps are expected to be as few as possible in device fabrication.

2. **Problem:** For the same device of problem 1, calculate the change in threshold voltage V_{T0} as the channel length is reduced from $1 \mu m$ to 60 nm .

Solution: For the same device of problem 1 with a channel length $L = 1 \mu m$, also using the device information given in problem 1 of HW6, i.e. AL gate with work function $e\phi_M = 3.0eV$ and the work function of Si substrate $e\chi = 3.2eV$, we have

$$\phi_B = 2 * \frac{k_B T}{e} \ln\left(\frac{N_a}{N_i}\right) = 2 \frac{1.38 \times 10^{23} \times 300}{1.6022 \times 10^{-19}} \ln\left(\frac{3 \times 10^{17}}{1.5 \times 10^{10}}\right) = 0.4344eV$$

and $V_{FB} = -0.3156eV$ (refer to solution of prob. 1 in HW6). From Eq. (300) we know that

$$\frac{Q_d}{Q_{d0}} = \frac{1}{2} \left(1 + \frac{L_1}{L}\right) = 0.53. \quad (6)$$

Then the reduction of the threshold voltage can be calculated using Eq. (301)

$$V_{T0,old} = V_{FB} + 2\phi_B + \frac{(4N_A e \epsilon_s \phi_B)^{1/2}}{c_{ox}} \times \frac{Q_d}{Q_{d0}} = 1.1eV. \quad (7)$$

3. **Problem:** Using the equation

$$L_G > G_F \left[W_{D,max} + \frac{\epsilon_{si}}{\epsilon_{ox}} t_{ox} \right], \quad (8)$$



estimate the minimum size (i.e., gate length L_G) of a device which will not exhibit short-channel effects. Assume the parameters of the two problems above and use a value of 5 for the 'geometric factor' G_F .

Solution: The depletion width can be calculated using Eq. (221)

$$\phi_B = \frac{k_B T}{e} \ln(N_A/N_i) = 0.4344,$$

$$W_{D,max} = \left[\frac{4\epsilon_s \phi_B}{e N_A} \right]^{1/2} = 61.15 \text{ nm}.$$

Therefore, the minimum gate length is

$$L_G = 5 \times [61.15 \times 10^{-9} + \frac{11.7}{3.9} \times 10^{-8}] = 0.46 \mu\text{m}. \quad (9)$$

4. **Problem:** (a) Repeat the calculation of the previous problem, but now assume $t_{ox} = 2 \text{ nm}$.
 (b) If we keep the same oxide thickness of 2 nm, what is the channel doping N_A required to scale the device to $L_G = 60 \text{ nm}$? Is this achievable? If so, would you want to use it? If not, why?

Solution: (a) With $t_{ox} = 2 \text{ nm}$, we can get $L_G = 0.34 \mu\text{m}$.

(b) From the equation in Prob. 3, we can get

$$W_{D,max} = \frac{L_G}{G_F} - \frac{\epsilon_{si}}{\epsilon_{ox}} \times t_{ox} = 6 \times 10^{-9}.$$

We can input the expression of $W_{D,max} = \sqrt{\frac{4\epsilon_s \phi_B}{e N_A}}$ into the above result and assume ϕ_B is unchanged.

Therefore, we can get

$$N_A = \frac{4\epsilon_s \phi_B}{e w_{D,max}^2} = 1.87 \times 10^{17}.$$



It is achievable, however, we would not use it in practice because the heavy doping in substrate and the thin oxide thickness will cause strong gate leakage. In addition, the heavily doping in substrate will also cause the reduction of electron mobility.

