



## ASIAN TEST SYMPOSIUM 2011

*November 21-23, 2011*

ATS 2011 is the twentieth in this series of symposia started in 1992 devoted to testing, fault tolerant computing and the design of reliable circuits and systems. ATS is recognized as the main event in Asia that covers the many dimensions of testing and fault-tolerance. In 2011, the 20<sup>th</sup> Anniversary of the Asian Test Symposium will be celebrated in New Delhi, India and is of particular significance due to the rise of Asia, over the last several decades, in the areas of integrated circuit design and manufacturing, and electronic systems and software engineering, both of which embrace testing as a core technology. New Delhi, in particular, is a major player in India's computing industry with emerging "technology satellites" in nearby Noida and Gurgaon and the face of her new "modernity". At the same time, New Delhi, is the centerpiece of Indian culture, tradition and cuisine, having been at the helm of Indian history for centuries, dating back to the Mughal period and the British Raj.

The theme for ATS 2011 will be "*Test Odyssey 2020: Testing Systems and Devices at the Peta and Nano Scales*". This theme is inspired by the fact that technology is trending towards extremely high levels of integration at the package and chip levels, very high speeds of operation (> 100 GHz) and use of deeply scaled technology (approaching 10nm CMOS). In addition, a key test challenge will arise due to the ability to design complex systems such as robots that encompass sensors, communications systems, processors, transducers and enabling software. In addition to passing post-manufacture test procedures, such systems and relevant devices must exhibit fault-tolerance and survivability characteristics.

**Topics of interest include (but are not limited to):** Original contributions in testing, fault tolerant and reliable computing are solicited. Topics of interest include, but are not limited to, the following categories:

Automatic Test Pattern Generation (ATPG)  
Test Compression  
Temperature/Power-aware Test  
Microprocessor Test  
Memory Test  
Test Quality and Reliability  
Fault Modeling/Defect Based Test  
Software Testing  
Other

Boundary Scan  
Online Test  
Design-for-testability (DFT)  
Mixed signal and Analog Test  
System-in-package (SiP)/ 3D Test  
Design Validation/Silicon Debug  
Fault Simulation/Diagnosis  
Board and System Test

The conference will feature invited keynotes, regular paper sessions, tutorials, panels, and industry track presentations. Call for proposals and submissions will follow soon. For panel, special session and industry track proposals contact the chairs below.

**GENERAL CHAIRS**  
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All special session submissions are also handled using the EasyChair system. Please choose from one of the following categories. For, industrial test practices paper guidelines is as above. Proposals related to panels/special sessions, embedded tutorials, and full/half day tutorials are limited to 3 pages, and should detail abstract and bulleted list of topics, targeted audience, proposed duration, organizer's name and affiliation, speakers' names, affiliations, short bios, and approval status for participation at ATS 2011.

*Innovative Industrial Test Practices*

*Special Session Proposal*

*Embedded Tutorial Proposal*

*Full/Half Day Tutorial Proposal*

**Important Dates:**

Papers	May 27, 2011
Special Session proposals	June 3, 2011
Tutorial proposals	June 3, 2011
Exhibition/Booth proposals	June 3, 2011
Notification of acceptance	August 1, 2011
Camera-ready paper due date	August 22, 2011

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For general information, contact the General Chairs  
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