

Final Exam Review ECE668 December, 2007

This review contains information about what you need to read and what type of questions you can get. Follow these guidelines. Don't hesitate to send me or the TA email if you have questions.

The Exam will be 1.5 hours and closed-book. For date and classroom, please review the class website. All materials covered in the classroom, even if not in textbook, are required for the exam. Also make sure that you check the homework problem and project. You can get questions that relate to them and the discussions we had in the classroom.

The exam will have similar format as the midterm.

Material: everything from the midterm. At most 25% of questions will be from midterm material. At least 75% of the questions will be from the new material.

New material is mainly from PPTs: compiler ILP, prefetching, process variation, and virtual memory related.

The exam questions will be of the following nature (note: list is not exhaustive):

- (1) Short questions. Requires a sentence or two as answers. What is the use of a TLB? Is prefetching good or bad for power? What are the main sources of power consumption in a pipeline? When is prefetching beneficial? What is an inverted page table? What is a page miss? Can you have a cache miss with no page miss? How is memory protection achieved? Difference between segmentation and paging. What is demand based paging? What is demand based segmentation? How do you prefetch sequential access patterns? What is different between array based and pointer based accesses for prefetching schemes? What is a logical address? How is translation done between physical and logical address spaces?
- (2) Problems that require analytical analysis/reasoning. For example, express the performance of a machine given some distribution of instructions and costs associated with different operations. Estimate power consumption. This could include various virtual memory organizations and physical/virtual caching schemes, and pipeline organizations, etc. I could use one of the examples from the slides for virtual memory/caching organization.
- (3) Compiler based ILP. Will show a segment of code and ask you to perform loop unrolling, register renaming, software pipelining and /or other scheduling optimizations. Understand VLIW/EPIC/OSI types of parallelism. Be able to point out when a superscalar design can win vs. a compiler-driven design.
- (4) Prefetching. Performance and power implications of various schemes. Why it works and what are the key issues such as cache pollution with untimely prefetch,

- unnecessary off-chip accesses, where power impact comes from, how can we optimize it, what are the hardware structures, etc.
- (5) Pipelining including Tomasulo and speculative Tomasulo. Understand how the original algorithm was modified to deal with speculation and precise interrupts.
 - (6) ILP Estimates. Have an architect's intuition for how ILP is lost with more realistic assumptions of the resources. All speculative techniques like branch prediction, prefetching, etc, can affect the IPC. How do they affect it?
 - (7) Process variation and schemes to address delay faults in the pipeline and memory system. How can BB be used? What are the key issues? Difference between environmental and physical variations. Intuition on how severe is the problem.
 - (8) Power consumption in pipelines. Calculate energy consumed in a program given some distribution of power in core architectural components and a simple pipeline structure. Assume using prefetching with certain architectural features and success rate in bringing in the correct cache lines ahead of their use.

The best way to prepare is to study the notes. Focus on understanding rather than memorizing when you study. We will review some more examples in class.

Good luck!

Professor Moritz