Introduction to Multi-Core

Baskaran Ganesan
Baskaran.ganesan@intel.com
Sr. Design Engineer
Digital Enterprise Group, Intel Corporation

Reach To Teach
Intel Higher Education Program &
Foundation for Advancement of Education and Research (FAER)
Topics

1. CPU (semiconductor) HISTORY (SESSION-1)
   a. Moore’s Law
   b. Transistor scaling
   c. Scaling limitations & impact
   d. What then?
      - Dual core
   e. The new era

- ARCHITECTURE (SESSION-2)
  a. Core Architecture
     - Core basics, Platform architecture, Core architecture
  b. Multi-core architecture
  c. Multi-core challenges
  d. Closing notes
Moore’s Law

“... the number of transistors on a chip approximately doubles every 24 months ...”

Gordon Moore
Circa 1975
Moore’s law at work

- Transistor Size
- Transistor Count
- CPU Arch technology
- Manufacturing technology
- Compute Power
- SW/IT eco-system
- Volume Market
- CPU Cost

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Historical Driving Forces

- **Shrinking Geometry**
  - Feature Size (um)
  - 1970 to 2020
  - 1971: 4004 Processor, 2300 Transistors
  - 1978: 8008 Processor, IBM PC
  - 1986: i386 Processor, 32-bit
  - 1993: Pentium Processor, 3.1M transistors
  - 2005: Montecito 1.7B Transistors

- **Increased Frequency**
  - Frequency (MHz)
  - 1970 to 2020
  - 1971: 4004 Processor
  - 1978: 8008 Processor
  - 1986: i386 Processor
  - 1993: Pentium Processor
  - 2005: Montecito 1.7B Transistors

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Scale Factors (loosely defined)

**Voltage scale-factor:** Rate at which the transistor voltage decreases with respect to a change in transistor dimensions.

**Frequency scale-factor:** Rate at which the transistor frequency increases with respect to a change in transistor dimensions.

**Cost scale-factor:** Rate at which the per-transistor cost decreases with respect to a change in transistor dimensions.

**Count scale-factor:** Rate at which the transistor count increases with respect to a change in transistor dimensions.
Scaling: More data
The Act of Balancing

Delivered Performance = Instructions Per Cycle (IPC) \times Frequency

Goal is higher performance and lower power

Power \propto C_{\text{dynamic}} \times V \times V \times Frequency
Scaling at its best

386 Processor

May 1986
@16 MHz core
275,000 1.5µ transistors
~1.2 SPECint2000

Pentium® 4 Processor

August 27, 2003
@3.2 GHz core
55 Million 0.13µ transistors
1249 SPECint2000

17 Years
200x
200x/11x
1000x

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Architectural Innovations

- Serial, sequential execution
- Overlapped execution (pipelining)
- Multi-stage, deep pipelining
- Control-speculative execution
- Data-speculative execution
- Super-scalar execution
- Out-of-order execution
- Vector computing
- Addressing extensions
- Application specific instructions
- Multi-level on-chip caching
- Memory disambiguation
- Register renaming
- Score-boarding
- Hardware data prefetching
- ...

Many decades of computer architecture focused on Instruction-Level Parallelism (ILP) enhancement
The Challenges

Power Limitations

Diminishing Voltage Scaling

Power = Capacitance × Voltage² × Frequency
also
Power ~ Voltage³
What then?

Performance
Power

Max Frequency

1.00x

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Over-clocking

- Over-clocked (+20%):
  - Performance: 1.73x
  - Power: 1.13x

- Max Frequency:
  - Performance: 1.00x
  - Power: 1.00x

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Under-clocking

- Over-clocked (+20%): 1.13x
- Max Frequency: 1.00x
- Under-clocked (-20%): 0.87x

Performance
Power

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Multi-Core Energy-Efficient Performance

- Over-clocked (+20%): 1.73x
- Max Frequency: 1.00x
- Dual-core (-20%): 1.02x

Relative single-core frequency and Vcc

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Dual core with voltage scaling

**RULE OF THUMB**

<table>
<thead>
<tr>
<th>Frequency Reduction</th>
<th>Power Reduction</th>
<th>Performance Reduction</th>
</tr>
</thead>
<tbody>
<tr>
<td>15%</td>
<td>45%</td>
<td>10%</td>
</tr>
</tbody>
</table>

A 15% Reduction In Voltage Yields

**SINGLE CORE**

- Area = 1
- Voltage = 1
- Freq = 1
- Power = 1
- Perf = 1

**DUAL CORE**

- Area = 2
- Voltage = 0.85
- Freq = 0.85
- Power = 1
- Perf = ~1.8

Performance Reduction

Power Reduction

Frequency Reduction

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Intel: Dual & Quad Cores

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A New Era...

The Old

Performance Equals Frequency
Unconstrained Power
Voltage Scaling

The New

Performance Equals IPC
Multi-Core
Power Efficiency
Microarchitecture Advancements

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Trade-off equations

- Power is costly; Transistors, relatively cheap
- Frequency alone is not important; Efficiency IS
- Performance-per-watt is critical; per-core performance is not quite
- Computation is relatively easy; Memory accesses are NOT
Q & A
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Typical PC Architecture

- Intel® Pentium® M Processor
  - AGP4x Interface (1.5V)
  - Intel® 855PM Chipset (MCH)
    - Hub Interface
    - 82855PM
    - DDR Memory
  - ICH4-M
    - ATA 100/66
      - 2 IDE Channels
    - 6 USB (2.0/1.1) Ports
    - AC97 Bus
    - Modem, Audio
    - PCI Bus
    - Cardbus
    - Intel® Pro/Wireless 2100 Network Connection

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Processor Resources

- Caches: L0, L1, L2 etc (Different levels of caches)
- General Purpose Registers (For SW programming)
- Segment Registers & TLB (for memory management)
- FP registers, XMM registers
- System Flags
- Control and Data registers, Debug registers, MSRs
- Many more
**CMP/SMP/HT**

**CMP:** Chip Multi Processing, refers to multiple physical core engines that have unique resources

- **Unique:** L0/L1 Cache, TLBs, Instruction Pointer, GP Regs
- **Shared:** L2 Cache

**SMP:** Refers to multiple threads that share all resources (time muxed)

- **Shared:** L0/L1/L2 Caches, TLBs
- **Unique:** Instruction Pointer, GP Regs

**Hyper Threading:** Refers to multiple threads that share more resources (L0/L1 Cache for example); May/May not be part of a CMP core

**SW Threading:** Application (SW) level threading of processes on one/more physical core engines
Core Architecture (Prescott)
Core Architecture (Xeon – Dual Core)
Multi-core platform (Freescale: embedded)

Freescale’s multicore Power platform will be built around the CoreNet fabric, which provides high throughput between memory, processing cores, and accelerators.
Multi-Core platform (RMI-XLR: embedded)
Tilera – 64 core CPU

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Tilera – Platform
Intel Polaris (80-core)
Tiled Design & Mesh Network

Repeated Tile Method:
- Compute + router
- Modular, scalable
- Small design teams
- Short design cycle

Mesh Interconnect:
- “Network-on-a-Chip”
  - Cores networked in a grid allows for super high bandwidth communications in and between cores
- 5-port, 80GB/s* routers
- Low latency (1.25ns*)
- Future: connect IA/or and special purpose cores
Multi-Core: what next?

100+ Research Projects Worldwide

**Microprocessor**
- **Examples:**
  - Scalable memory
  - Multi-core architectures
  - Specialized cores
  - Scalable fabrics
  - Energy efficient circuits

**Platform**
- **Examples:**
  - 3D Stacked Memory
  - Cache Hierarchy
  - Virtualization/Partitioning
  - Scaleable OS’s
  - I/O & Networking

**Programming**
- **Examples:**
  - Speculative Multithreading
  - Transactional memory
  - Workload analysis
  - Compilers & Libraries
  - Tools

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Connecting multiple cores

**Bi-directional Ring**

**Mesh**

**Hierarchical Rings (2deep)**

**Torus**

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Platform Architecture (multi-core)
Multi-core: Architectural Challenges

- Instruction-level parallelism v/s Thread-level parallelism tradeoffs and balance
- Shared resource management (functional units, caches, tlb, btb)
- Multi-threading v/s Multi-core tradeoffs
- On and Off-chip bandwidth requirements
- Latencies (execution, cache, and memory) reduction
- Memory Coherence/Consistency (for high speed on-die cache hierarchies)
- Multiple domains (and crossing) in clocking, voltage, reset,…
- Partitioning resources (between threads/cores)
- Fault tolerance (at device, storage, execution, core level) (aka reliability)
- On-die interconnect (optimized along latency, bw, modularity, power, …)
- Integration (of system components, and/or fixed function devices)
Multi-core: Design Challenges

Design Complexity, Productivity Tools / Methods Advance
• ...But at slower rate than Moore’s Law
• Replicating cores improves productivity

Visibility for Test & Debug
• Pin Bandwidth/Transistor continues to decline
• Shrinking dimensions, increasing speeds, ...
• Increased test time adding to cost

Power
• Power Delivery – di/dt of Amps/nano-second
• Thermals: Overall power and thermal density
Multi-core: Eco-system challenges

Underlying Software assumptions on resource sharing
• Lack of standard mechanisms to share “resource sharing info” between hw and OS

Lack of “Resource sharing” aware SW
• Compilers, Schedulers, Configuration/Management (Power!) etc

Legacy SW architectural requirements left on Multi-Core CPUs
• Compatibility requirements

Many more...unknowns (to CPU Design world)
Multi-core: Software Challenges

- Scalability of O/S Data Structures and Policies
  - Synchronization and locking, Scheduling, Process management, Data structure sizing and management limitations, Threading granularity and primitives

- Memory Hierarchy Awareness
  - Impact of coherency policy, Efficiency of Data-sharing and Process migration effects, SW visibility to High speed on-die interconnect, SW control of Cache hierarchy, NUCA Awareness

- High Bandwidth I/O Support
  - Light weight Interrupts, Data movement and transformation engines, I/O Affinity

Algorithms, Programming Languages, Compilers, Operating Systems, Architectures, Libraries, … not ready for 100s of CPUs / chip
More than the cores

![Graph showing performance increase with different numbers of cores]

- New instructions
- Cache improvements
- HW thread scheduling
- Baseline

Value of Tera-scale Research
Just Adding Cores

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Closing notes

• Single and Multi-core architectures presented
• Multi-Core CPU is the next generation CPU Architecture
  – 2Core and Intel Quad-Core designs plenty on market already
  – Many More are on their way
• Several old paradigms ineffective; Several new problems to be addressed
• Chip Level Multiprocessing and large caches can exploit Moore’s Law
• Thread/Core count in future microprocessor systems to increase
• Eco-system immature/non-existent
• Numerous domains in arch/design awaiting research & innovation and here is where you come in!!!
Acknowledgements

Gautam Doshi [Principal Engineer, Digital Enterprise Group]
Ajay Bhatt [Intel Fellow, Digital Enterprise Group]
Dileep Bhandarkar [Architect, Digital Enterprise Group]
Sunit Tyagi [Sr. Principal Engineer, Digital Enterprise Group]
... and countless foil-wares
Resources

Intel Core Microarchitecture:  http://www.intel.com/technology/architecture/coremicro/
Multi/Many Core:  http://www.intel.com/multi-core/index.htm
Backup: Core uArch
Intel® Core™ Microarchitecture

- Low Power
  - Intel® Wide Dynamic Execution
  - Intel® Intelligent Power Capability
  - Intel® Advanced Smart Cache
  - Intel® Smart Memory Access
  - Intel® Advanced Digital Media Boost

- High Performance
  - Server Optimized
  - Desktop Optimized
  - Mobile Optimized

- Scalable
  - (Xeon) Woodcrest
  - (Core2 Duo) Conroe
  - (Core2 Duo) Merom

65nm

*Graphics not representative of actual die photo or relative size

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Intel® Intelligent Power Capability

- **Process**
  - 65nm
  - Strained Silicon
  - Low-K Dielectric
  - More Metal Layers

- **Coarse Grained**
  - Aggressive Clock Gating
  - Enhanced Speed-Step

- **Ultra Fine Grained**
  - Low VCC Arrays
  - Blocks Controlled Via Sleep Transistors

- **Transistor**
  - Low Leakage Transistors
  - Sleep Transistors

**ADVANTAGE**
- Mobile-Level Power Management
- Energy Efficient Performance

*Graphics not representative of actual die photo or relative size*

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Intel® Wide Dynamic Execution

**EACH CORE**

- **EFFICIENT**
  - 14 STAGE PIPELINE
- **DEEPER BUFFERS**
- **4 WIDE - DECODE TO EXECUTE**
- **4 WIDE - MICRO-OP EXECUTE**
- **MICRO and MACRO FUSION**
- **ENHANCED ALUs**

**ADVANTAGE**

- 33% Wider Execution over Previous Gen
- Comprehensive Advancements
- Enabled In Each Core

**Core 1**

- INSTRUCTION FETCH AND PRE-DECODE
- INSTRUCTION QUEUE
- DECODE
- RETIREMENT UNIT (REORDER BUFFER)
- SCHEDULERS
- EXECUTE

**Core 2**

- INSTRUCTION FETCH AND PRE-DECODE
- INSTRUCTION QUEUE
- DECODE
- RETIREMENT UNIT (REORDER BUFFER)
- SCHEDULERS
- EXECUTE
## Intel® Wide Dynamic Execution

### Micro and Macro Fusion

<table>
<thead>
<tr>
<th>WITH MACRO FUSION</th>
<th>WITHOUT MACRO FUSION</th>
</tr>
</thead>
<tbody>
<tr>
<td>INSTRUCTION 3</td>
<td>INSTRUCTION 3</td>
</tr>
<tr>
<td>INSTRUCTION 2</td>
<td>INSTRUCTION 2</td>
</tr>
<tr>
<td>INSTRUCTION 1</td>
<td>INSTRUCTION 1</td>
</tr>
<tr>
<td>DECODE</td>
<td>DECODE</td>
</tr>
<tr>
<td>COMBINED INST 2 &amp; 3</td>
<td>INTERNAL INST 3</td>
</tr>
<tr>
<td>INTERNAL INST 1</td>
<td>INTERNAL INST 2</td>
</tr>
<tr>
<td>EXECUTE</td>
<td>EXECUTE</td>
</tr>
<tr>
<td>COMPLETED INST 3</td>
<td>COMPLETED INST 3</td>
</tr>
<tr>
<td>COMPLETED INST 2</td>
<td>COMPLETED INST 2</td>
</tr>
<tr>
<td>COMPLETED INST 1</td>
<td>COMPLETED INST 1</td>
</tr>
</tbody>
</table>

**ADVANTAGE**

- Instruction Load Reduced ~ 15%**
- Micro-Ops Reduced ~ 10%**

*Graphics not representative of actual die photo or relative size

** Workload dependant

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Intel® Advanced Smart Cache
Dynamic L2 Cache Usage

Core™ Microarchitecture
Shared L2

Increased Traffic
Decreased Traffic

Dynamically, Bi-Directionally Available

Independent L2
Not Shareable

L1 CACHE
L1 CACHE

L1 CACHE
L1 CACHE

CORE 1
CORE 2
CORE 1
CORE 2

ADVANTAGE
• Higher Cache Hit Rate
• Reduced BUS Traffic
• Lower Latency to Data

Energy
Perf

*Graphics not representative of actual die photo or relative size
Intel® Smart Memory Access
Hardware-based Memory Disambiguation

Core™ Microarchitecture

- INST 2 “LOAD [Y]”
- INST 1 “STORE [X]”

IN ORDER

DECODE/SCHEDULE

INST 2 “LOAD [Y]”
INST 1 “STORE [X]”

OUT OF ORDER

EXECUTE

INST 2 “LOAD [Y]”
INST 1 “STORE [X]”

HARDWARE Mem. Dis. Predictor

Inst. 2 “Load” Can Occur Before Inst. 1 “Store”

Other

- INST 2 “LOAD [Y]”
- INST 1 “STORE [X]”

IN ORDER

DECODE/SCHEDULE

INST 2 “LOAD [Y]”
INST 1 “STORE [X]”

OUT OF ORDER

EXECUTE

INST 1 “STORE [X]”

STALL

Inst. 2 Must Wait For Inst. 1 “Store” To Complete

Perf

ADVANTAGE

• Higher Utilization of Pipeline
• Masks latency to data access
• Higher Performance

Energy

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Intel® Advanced Digital Media Boost
Single Cycle SSE

In Each Core
- Fusion Support
- Single Cycle SSE
- DECODE
- EXECUTE

SSE Operation (SSE/SSE2/SSE3)
- SOURCE
- X4
- X3
- X2
- X1
- SSE/2/3 OP
- Y4
- Y3
- Y2
- Y1
- DEST
- X4opY4
- X3opY3
- X2opY2
- X1opY1

Core™ μarch
- CLOCK CYCLE 1
- X4opY4 X3opY3 X2opY2 X1opY1

Previous
- CLOCK CYCLE 1
- X2opY2 X1opY1
- CLOCK CYCLE 2
- X4opY4 X3opY3

ADVANTAGE
- Increased Performance
- 128 bit Single Cycle in each core
- Improved Energy Efficiency

*Graphics not representative of actual die photo or relative size

Perf ↑
Energy ↓

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Backup: Next Gen Technologies
Traditional Operating Systems (Time-mux)

Applications interface with the operating system:
- Application 1
- Application 2
- Application 3
- Application 4

The operating system controls the hardware platform, and isolates applications from hardware:
- BIOS
- UEFI
- ACPI
- PCI Cfg

Device drivers have direct access to the hardware devices that they control.

PC Platform
What is Virtualization?

Without VMs: Single OS owns all hardware resources

With VMs: Multiple OSes share hardware resources

Virtualization enables multiple operating systems to run on the same platform

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Types of Virtualization

Hosted VMM
• launched from within an OS, e.g., VMplayer, WSX, GSX, Virtual PC, Virtual Server
  – Cheap but lower performance

Hypervisor: A bootable layer on Bios
• Thick: embeds all the drivers, e.g., ESX
• Thin: has a service VM, e.g., Xen derivates

Virtual Appliances: dedicated Virtual machines, e.g., MojoPC
Intel® Virtualization Technology (VT)

**Intel® VT**
First to market with native virtualization support
Broadest HW and SW ecosystem support

**Core™ Microarchitecture based systems**
- Significant increase in performance and improved VT performance overall segments
  - Mobile - Intel® Core™2 Duo Mobile Processor for Intel® Centrino® Duo Mobile Technology
  - Desktop - Intel® Core™2 Duo Desktop Processor E6000 sequence -
  - Server Dual and Quad Core Intel® Xeon® Processor 5000 series

Get More Done On Every Server
Get More Capabilities On Client
Trusted Execution Technology

- Standard
  - Apps
  - OS
- Protected
  - applet
  - kernel

Protected Memory

Domain Manager

LT CPU + LT C/S + Protected I/O + TPM

LaGrande Technology

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LT Hardware Ingredients

LT = CPU + Chipset + TPM + Protected I/O

CPU Extensions
✓ Enables domain separation
✓ Sets policy for protected memory

Protected Graphics
✓ Trusted channel between graphics and trusted SW
✓ Integrated or third party discrete graphics

Protected Keyboard & Mouse
✓ Trusted channel between keyboard/mouse and trusted SW

Protected Memory Mgmt
✓ Enforces access policy to protected memory

Trusted Platform Module v1.2
✓ Protects keys, digital certificates & attestation credentials
✓ Provides platform authentication
Backup: Misc
Moore’s Law Moving Forward

|-----------------------------|ACTUAL-----------------------------|FORECAST-|
|Production                  | 1995 1997 1999 2001 2003 2005 2007 2009 2011 |
|Generation                  | 0.35 0.25 0.18 130\text{nm} 90\text{nm} 65\text{nm} 45\text{nm} 35\text{nm} 22\text{nm} |
|Gate Length                 | 0.35 0.20 0.13 <70\text{nm} <50\text{nm} <35\text{nm} <35\text{nm} <35\text{nm} <22\text{nm} |
|Wafer Size (\text{mm})      | 200 200 200 300 300 300 300 300? 300? |
|Integration Capacity        | <100M 100M 200M 500M 1B >1B >2B >4B >8B |

“Another decade is probably straight-forward ... There is certainly no end to creativity.”

- Gordon Moore, speaking of extending Moore’s Law at ISSCC, Feb 2003
Multi-Core Power Efficiency

Many core is more power efficient

Power ~ area

Single thread performance ~ area^{0.5}

Power = \frac{1}{4}

Performance = \frac{1}{2}
Multi-Core and Memory Gap

Growing Performance Gap

Peak Instructions Per DRAM Access

Reduce DRAM access with large caches
    Extra benefit: power savings. Cache is lower power than logic

Tolerate memory latency with multiple threads
    Multiple cores
    Hyper-threading
Multi-threading tolerates memory latency

Serial Execution

Multi-threaded Execution

Execute thread B while thread A waits for memory

Multi-core has a similar effect
Multi-core tolerates memory latency

Serial Execution

\[ A_i \quad \text{Idle} \quad A_{i+1} \quad B_i \quad \text{Idle} \quad B_{i+1} \]

Multi-core Execution

\[ A_i \quad \text{Idle} \quad A_{i+1} \]
\[ B_i \quad \text{Idle} \quad B_{i+1} \]

Execute thread A and B simultaneously
How does Multicore Change Parallel Programming?

No change in fundamental programming model

Synchronization and communication costs greatly reduced
• Makes it practical to parallelize more programs

Resources now shared
• Caches
• Memory interface
• Optimization choices may be different
Art of the Possible

Billion transistors realized in 65nm Si process

Multi-Billion transistors possible in future Si process

Large die sizes can be built
  – 400 to 600 square millimeters

What can fit on a single die?
  – For 65nm (rough est)
    • 30 mm² per proc.
    • 15 mm² per MB

<table>
<thead>
<tr>
<th>Die size (core + cache only) in mm²</th>
<th>2 cores</th>
<th>4 cores</th>
<th>8 cores</th>
</tr>
</thead>
<tbody>
<tr>
<td>16 MB cache</td>
<td>300</td>
<td>360</td>
<td>480</td>
</tr>
<tr>
<td>32 MB cache</td>
<td>540</td>
<td>600</td>
<td>720</td>
</tr>
</tbody>
</table>
Quad Cores – here a quarter ago already!

Intel quad-core sales surpass 1m, chip maker claims

By Tony Smith → More by this author
2 Jul 2007 10:11
And that's just the ones for servers

Intel has sold more than a million quad-core processors, the company claimed late last week, making good its pledge made in September 2006 to beat that target before arch-rival AMD sells just one quad-core server chip.

AMD’s four-core 'Barcelona' processor’ won't appear until August, the chip maker said last week.

Intel representatives in the US and Asia made the million-chip claim, which specifically centres on the giant's Xeon 5300 'Clovertown' server processor - the Core 2 Extreme and Core 2 Quad CPUs it's sold push the total even higher, but probably not much higher.

Intel's own projections don’t envisage demand for desktop quad-core chips to hit ten per cent of its desktop processor sales in Q3.
Multi-Core

Intel’s Polaris prototype is a glimpse ten years into chip futures

Posted by Jesse D. Lewin on Jan 17th at 1:55 PM

Our new favorite phrase in hardware lust around the 10 HQ has been 'multi-core' (Sampy says it like Leeloo Dallas says 'multi-pass'). However according to Intel's CTO the era of many-core isn't so far off. Justin Rattner tested the first Polaris processor prototypes recently, and he's pleased to report that deep inside Intel's test labs, they were getting 1.02 TFLOPS at 3.2GHz, all for less than 100 watts of power. Justin would also remind you that a decade ago, that sort of power took up a space about the size of your house.

The full specs of the Polaris chip are available, and there's certainly no roadmap for putting these bad boys on the shelves at Fry's. Nonetheless, these sort of lab accomplishments send shockwaves through our minds. If you want a good job in 2020, start learning how to program to as many cores as you can imagine.

Tags: future, hardware, Intel